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SECTION 1. GENERAL

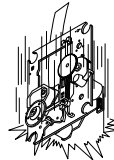
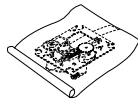
❑ SERVICING PRECAUTIONS

NOTES REGARDING HANDLING OF THE PICK-UP

1. Notes for transport and storage

- 1) The pick-up should always be left in its conductive bag until immediately prior to use.
- 2) The pick-up should never be subjected to external pressure or impact.

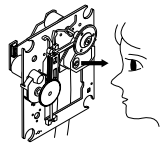
Storage in conductive bag



Drop impact

2. Repair notes

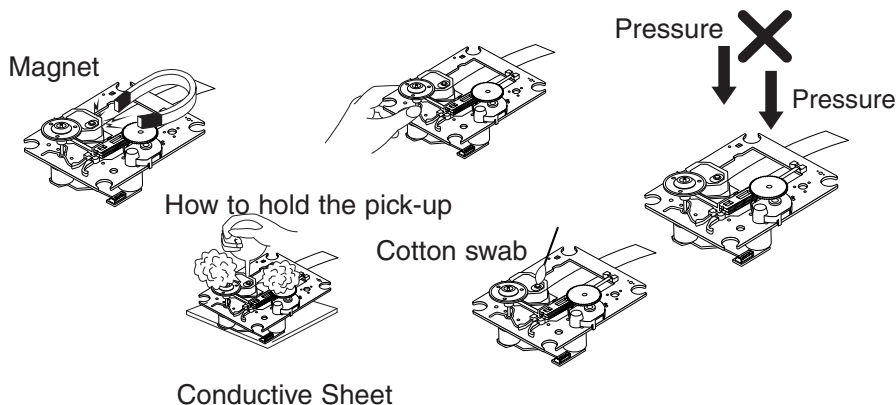
- 1) The pick-up incorporates a strong magnet, and so should never be brought close to magnetic materials.
- 2) The pick-up should always be handled correctly and carefully, taking care to avoid external pressure and impact. If it is subjected to strong pressure or impact, the result may be an operational malfunction and/or damage to the printed-circuit board.
- 3) Each and every pick-up is already individually adjusted to a high degree of precision, and for that reason the adjustment point and installation screws should absolutely never be touched.
- 4) Laser beams may damage the eyes!
Absolutely never permit laser beams to enter the eyes!
Also NEVER switch ON the power to the laser output part (lens, etc.) of the pick-up if it is damaged.



NEVER look directly at the laser beam, and don't let contact fingers or other exposed skin.

5) Cleaning the lens surface

If there is dust on the lens surface, the dust should be cleaned away by using an air bush (such as used for camera lens). The lens is held by a delicate spring. When cleaning the lens surface, therefore, a cotton swab should be used, taking care not to distort this.



6) Never attempt to disassemble the pick-up.

Spring by excess pressure. If the lens is extremely dirty, apply isopropyl alcohol to the cotton swab. (Do not use any other liquid cleaners, because they will damage the lens.) Take care not to use too much of this alcohol on the swab, and do not allow the alcohol to get inside the pick-up.

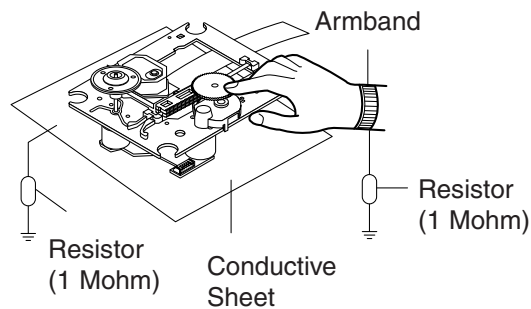
NOTES REGARDING COMPACT DISC PLAYER REPAIRS

1. Preparations

- 1) Compact disc players incorporate a great many ICs as well as the pick-up (laser diode). These components are sensitive to, and easily affected by, static electricity. If such static electricity is high voltage, components can be damaged, and for that reason components should be handled with care.
- 2) The pick-up is composed of many optical components and other high-precision components. Care must be taken, therefore, to avoid repair or storage where the temperature of humidity is high, where strong magnetism is present, or where there is excessive dust.

2. Notes for repair

- 1) Before replacing a component part, first disconnect the power supply lead wire from the unit
- 2) All equipment, measuring instruments and tools must be grounded.
- 3) The workbench should be covered with a conductive sheet and grounded.
When removing the laser pick-up from its conductive bag, do not place the pick-up on the bag. (This is because there is the possibility of damage by static electricity.)
- 4) To prevent AC leakage, the metal part of the soldering iron should be grounded.
- 5) Workers should be grounded by an armband (1M Ω)
- 6) Care should be taken not to permit the laser pick-up to come in contact with clothing, in order to prevent static electricity changes in the clothing to escape from the armband.
- 7) The laser beam from the pick-up should NEVER be directly facing the eyes or bare skin.



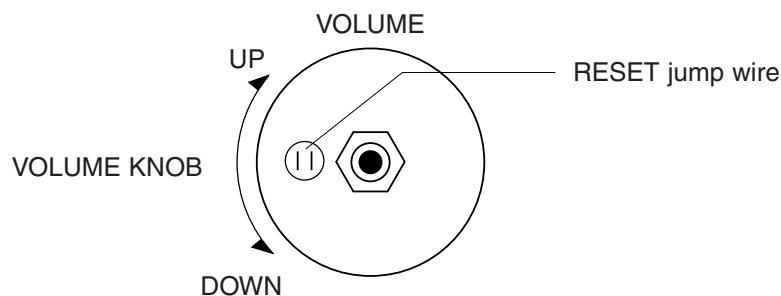
CLEARING MALFUNCTION

You can reset your unit to initial status if malfunction occur(button malfunction, display, etc.).

Using a pointed good conductor(such as driver), simply short the RESET jump wire on the inside of the volume knob for more than 3 seconds.

If you reset your unit, you must reenter all its settings(stations, clock, timer)

- NOTE:**
1. To operate the RESET jump wire, pull the volume rotary knob and release it.
 2. If you wish to operate the RESET jump wire, it is necessary to unplug the power cord.



❑ ESD PRECAUTIONS

Electrostatically Sensitive Devices (ESD)

Some semiconductor (solid state) devices can be damaged easily by static electricity. Such components commonly are called Electrostatically Sensitive Devices (ESD). Examples of typical ESD devices are integrated circuits and some field-effect transistors and semiconductor chip components. The following techniques should be used to help reduce the incidence of component damage caused by static electricity.

1. Immediately before handling any semiconductor component or semiconductor-equipped assembly, drain off any electrostatic charge on your body by touching a known earth ground. Alternatively, obtain and wear a commercially available discharging wrist strap device, which should be removed for potential shock reasons prior to applying power to the unit under test.
2. After removing an electrical assembly equipped with ESD devices, place the assembly on a conductive surface such as aluminum foil, to prevent electrostatic charge buildup or exposure of the assembly.
3. Use only a grounded-tip soldering iron to solder or unsolder ESD devices.
4. Use only an anti-static solder removal device. Some solder removal devices not classified as "anti-static" can generate electrical charges sufficient to damage ESD devices.
5. Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ESD devices.
6. Do not remove a replacement ESD device from its protective package until immediately before you are ready to install it. (Most replacement ESD devices are packaged with leads electrically shorted together by conductive foam, aluminum foil or comparable conductive materials).
7. Immediately before removing the protective material from the leads of a replacement ESD device, touch the protective material to the chassis or circuit assembly into which the device will be installed.

CAUTION : BE SURE NO POWER IS APPLIED TO THE CHASSIS OR CIRCUIT, AND OBSERVE ALL OTHER SAFETY PRECAUTIONS.

8. Minimize bodily motions when handling unpackaged replacement ESD devices. (Otherwise harmless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity sufficient to damage an ESD device).

CAUTION. GRAPHIC SYMBOLS

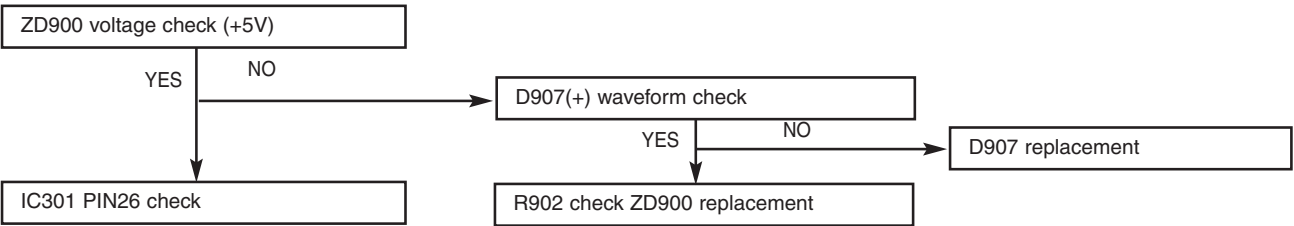
	THE LIGHTNING FLASH WITH ARROWHEAD SYMBOL. WITHIN AN EQUILATERAL TRIANGLE, IS INTENDED TO ALERT THE SERVICE PERSONNEL TO THE PRESENCE OF UNINSULATED "DANGEROUS VOLTAGE" THAT MAY BE OF SUFFICIENT MAGNITUDE TO CONSTITUTE A RISK OF ELECTRIC SHOCK.
	THE EXCLAMATION POINT WITHIN AN EQUILATERAL TRIANGLE IS INTENDED TO ALERT THE SERVICE PERSONNEL TO THE PRESENCE OF IMPORTANT SAFETY INFORMATION IN SERVICE LITERATURE.

MEMO

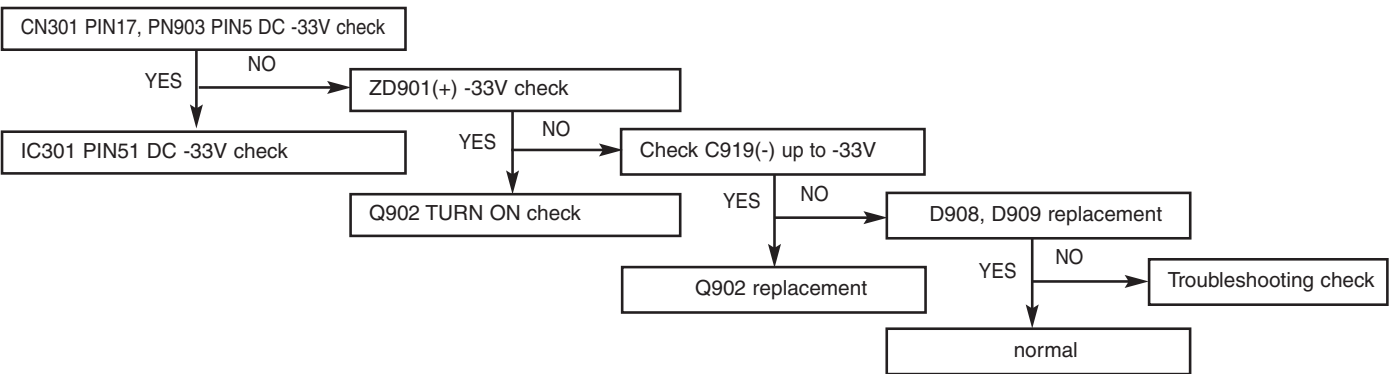
SECTION 2. ELECTRICAL

□ TROUBLESHOOTING GUIDE

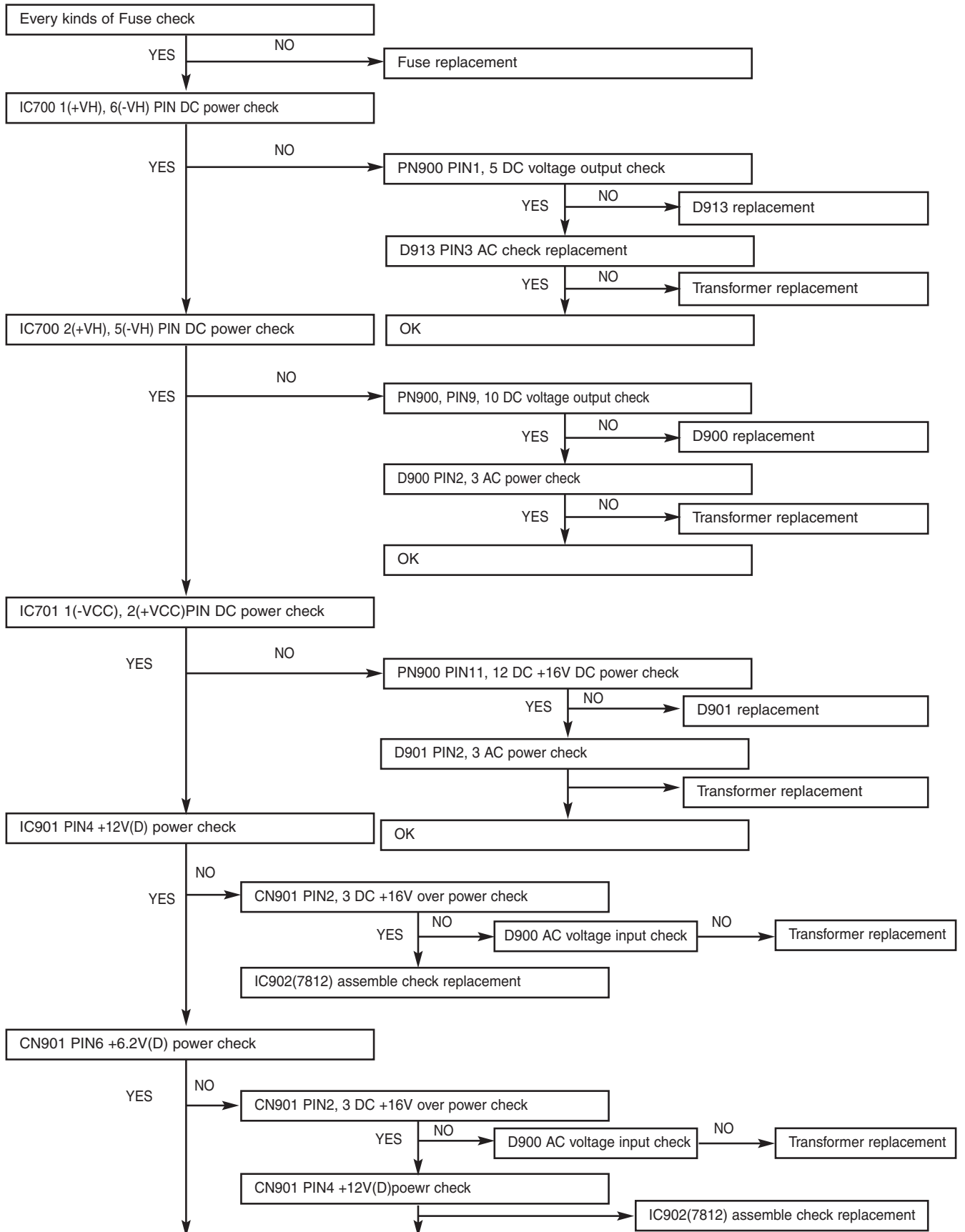
P-SENS CHECK

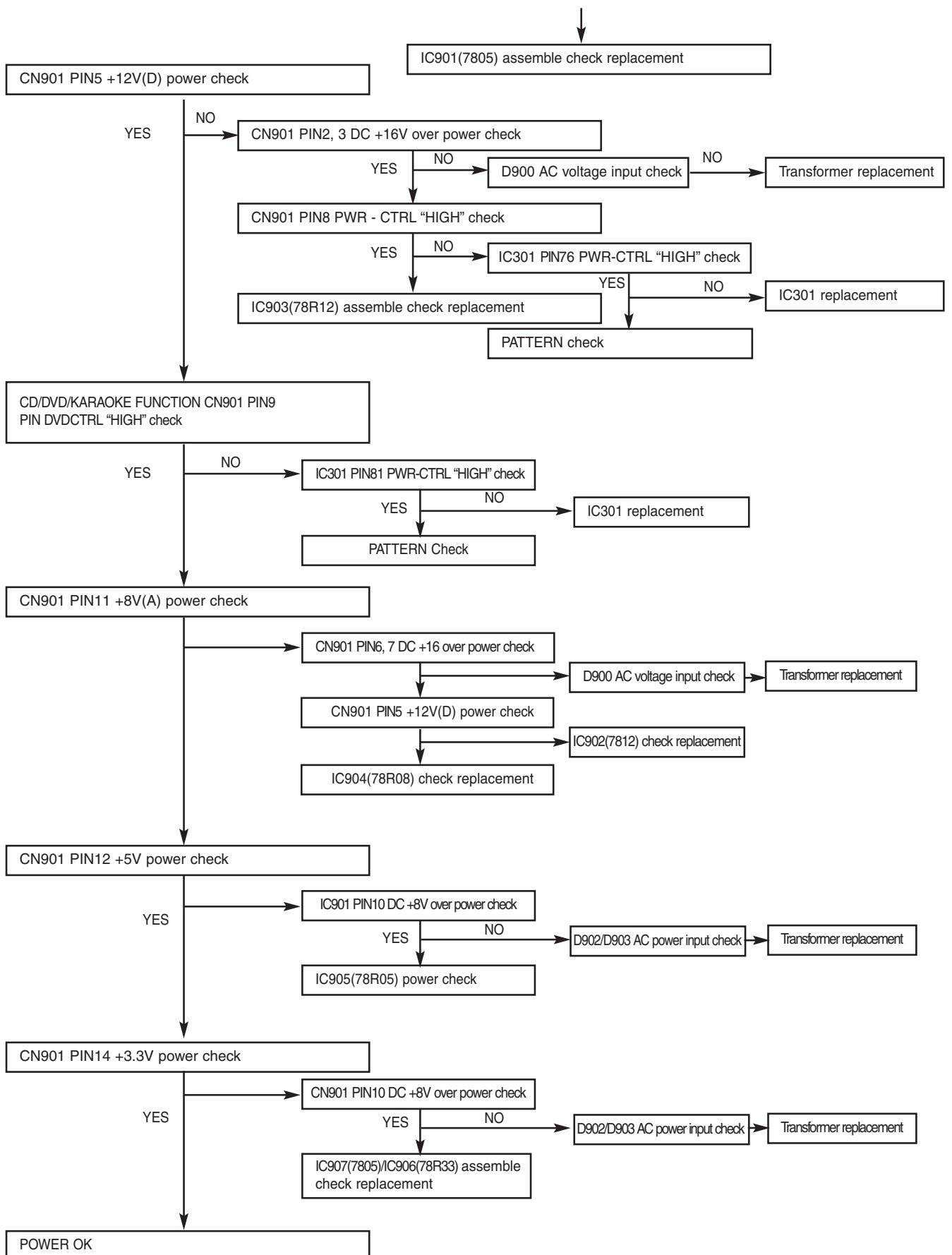


VKK CHECK

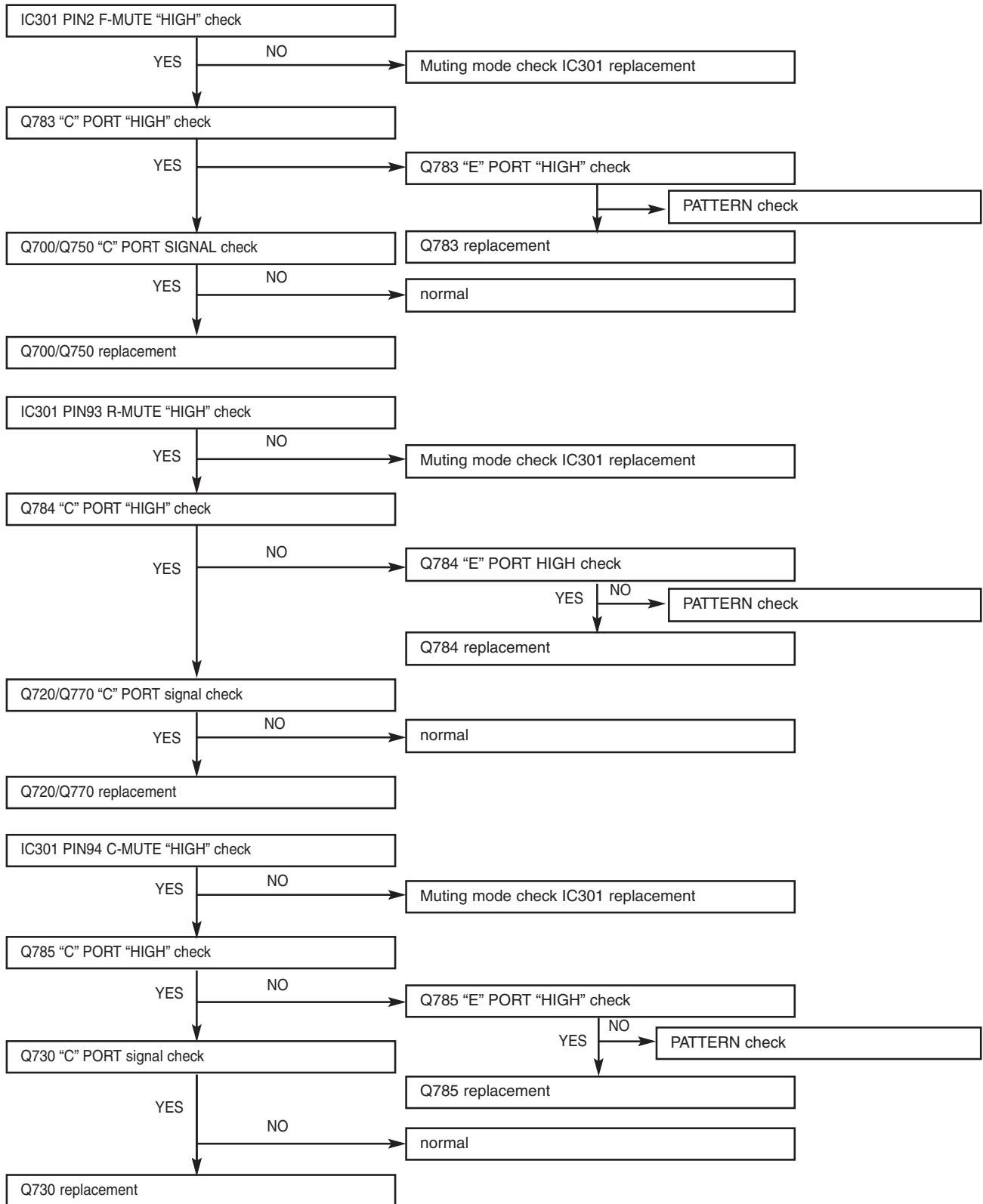


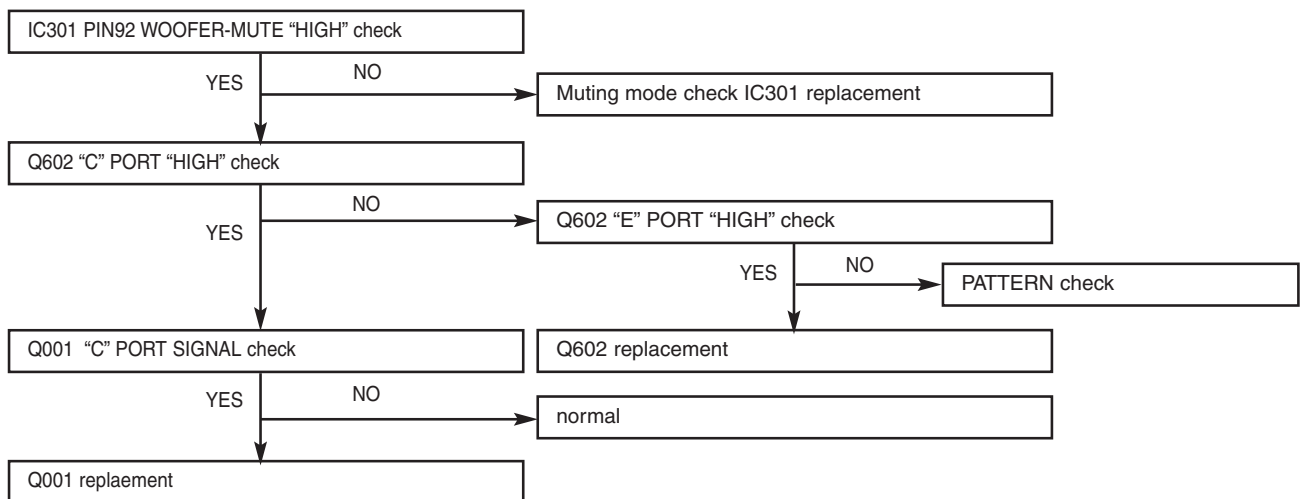
POWER CHECK



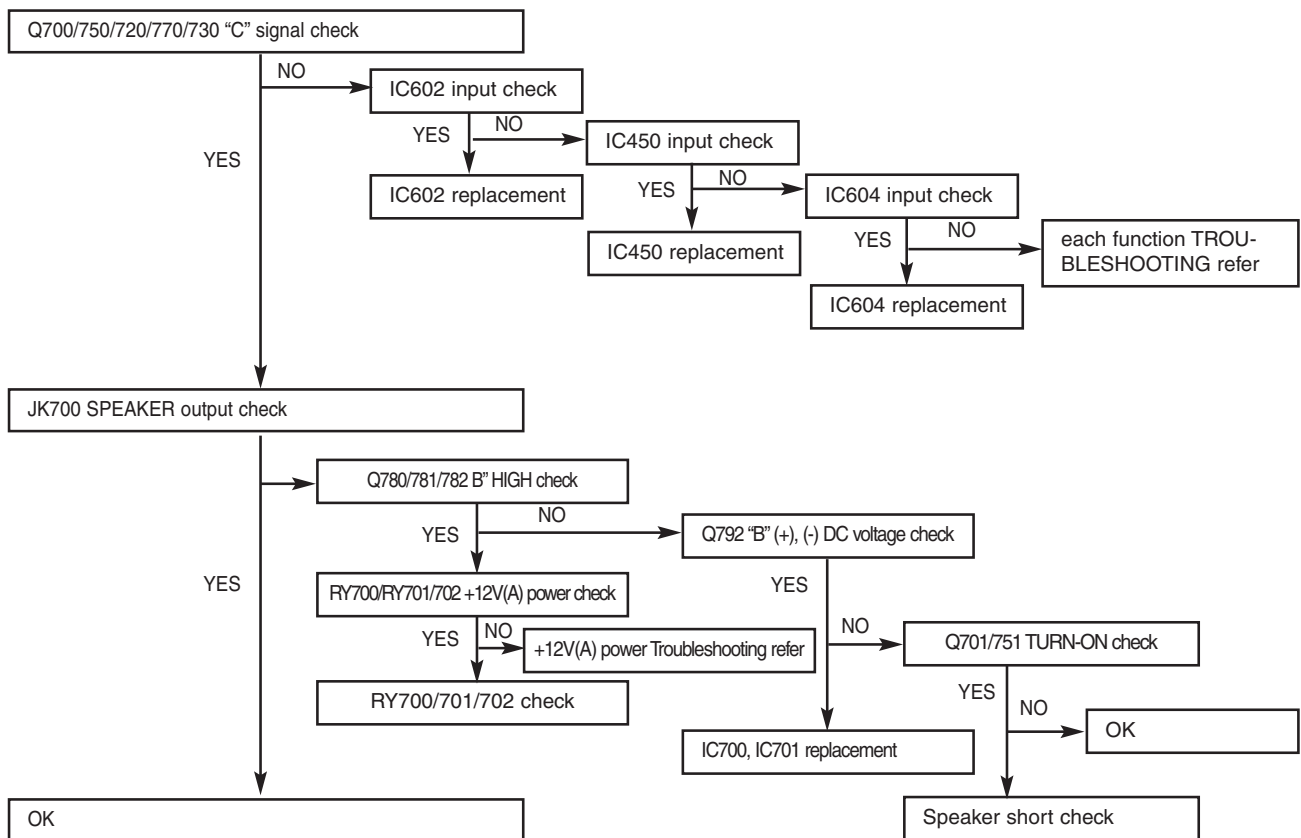


Muting circuit Troubleshooting (if MUTE)

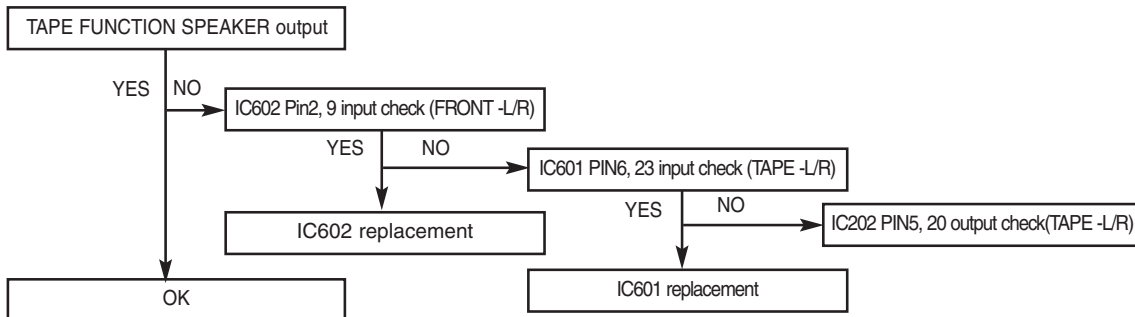
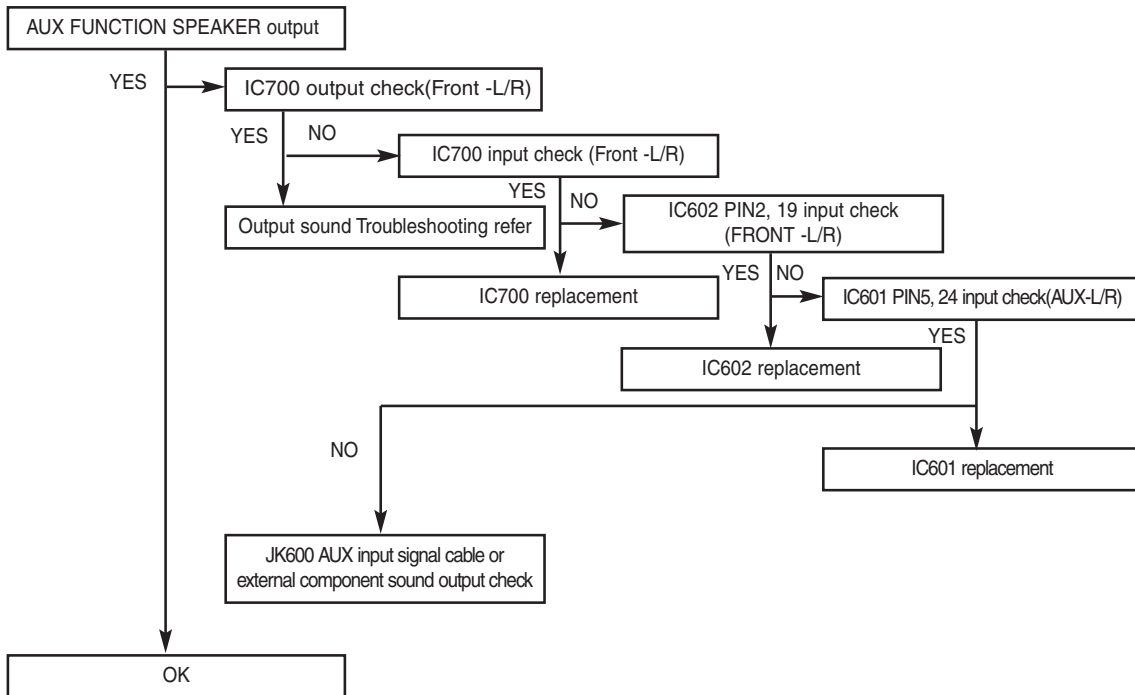


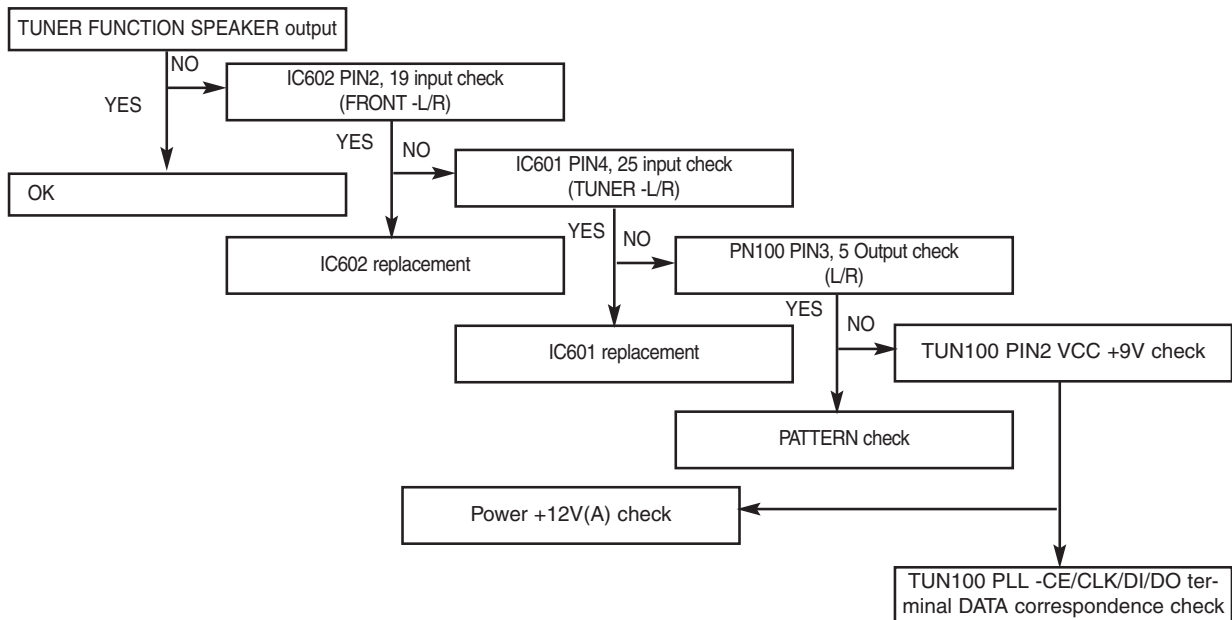
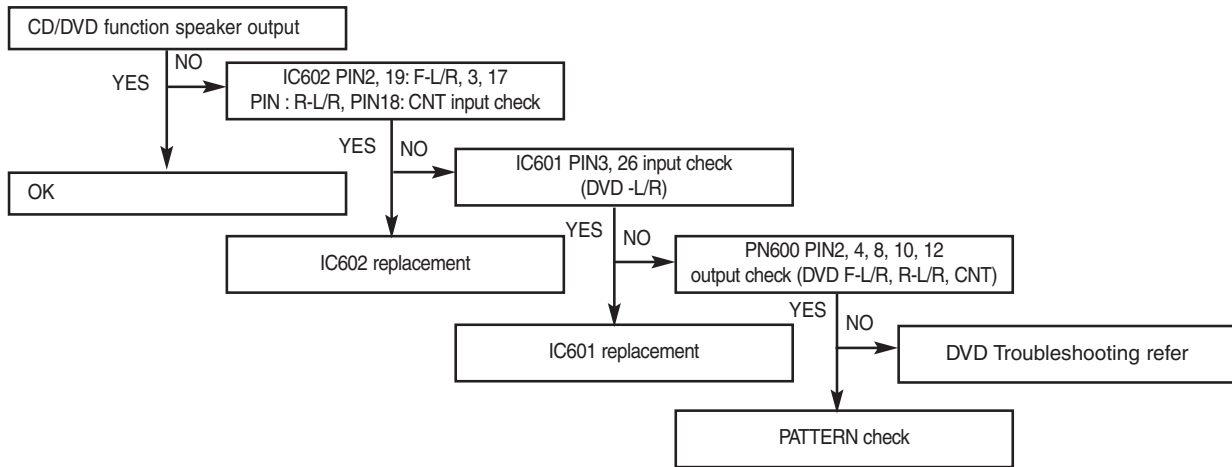


no sound

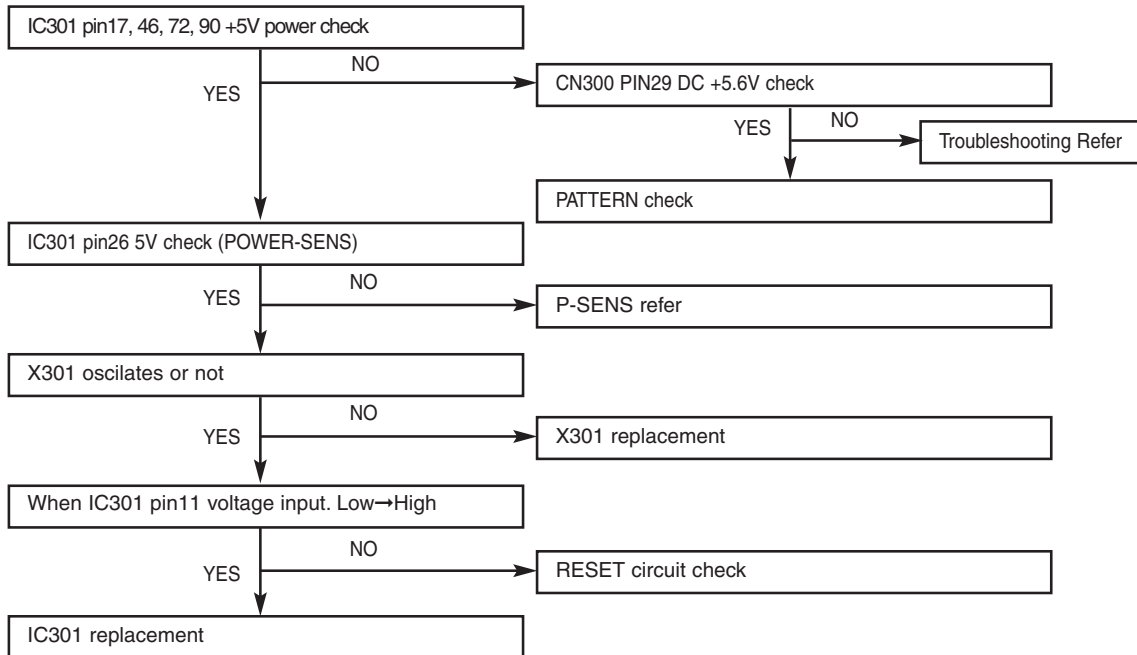


Specific FUNCTION MODE has no sound

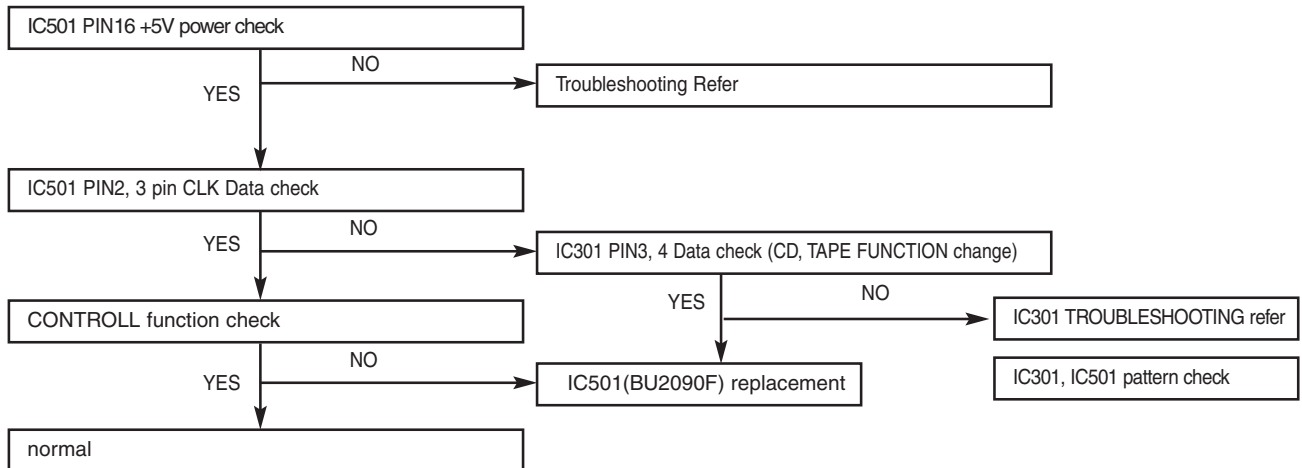




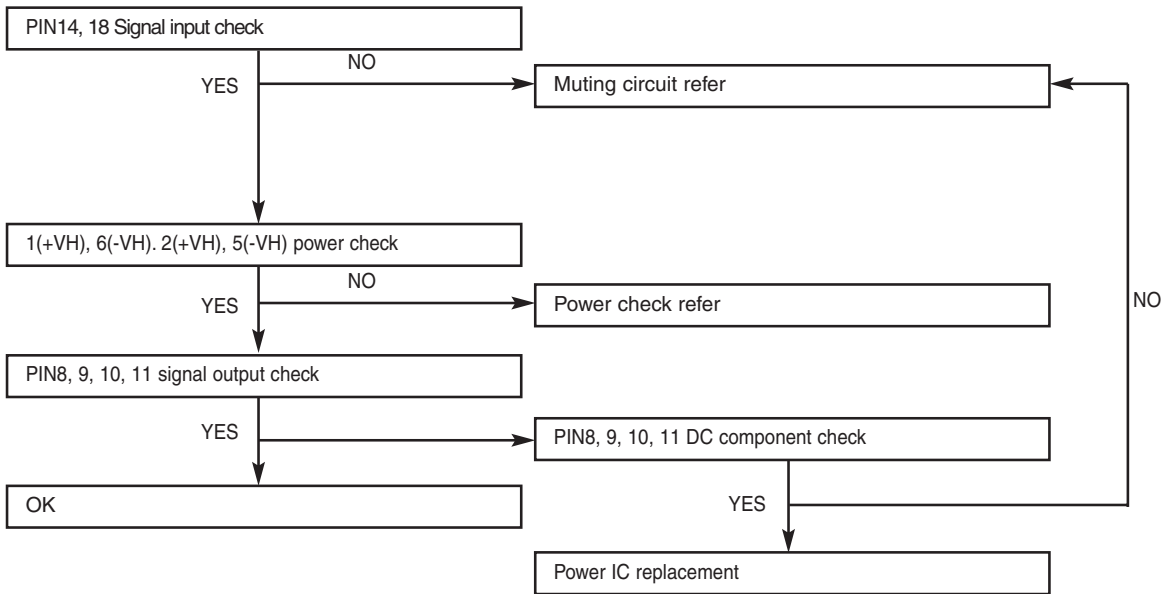
IC301 U-COM IC Troubleshooting



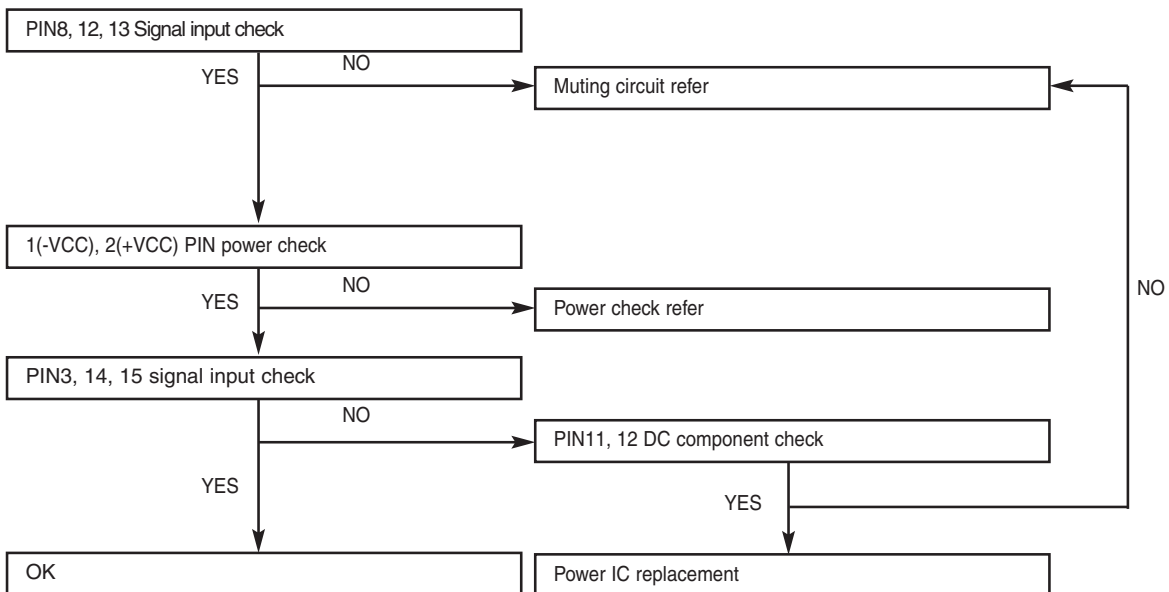
IC501(EXPENDER IC) Troubleshooting



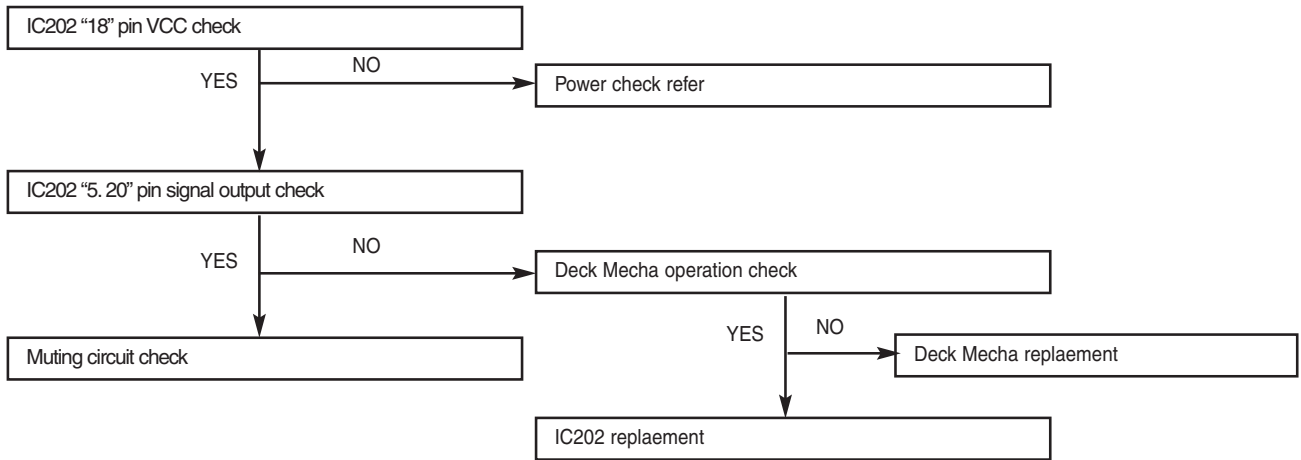
IC700(AMP IC) Troubleshooting



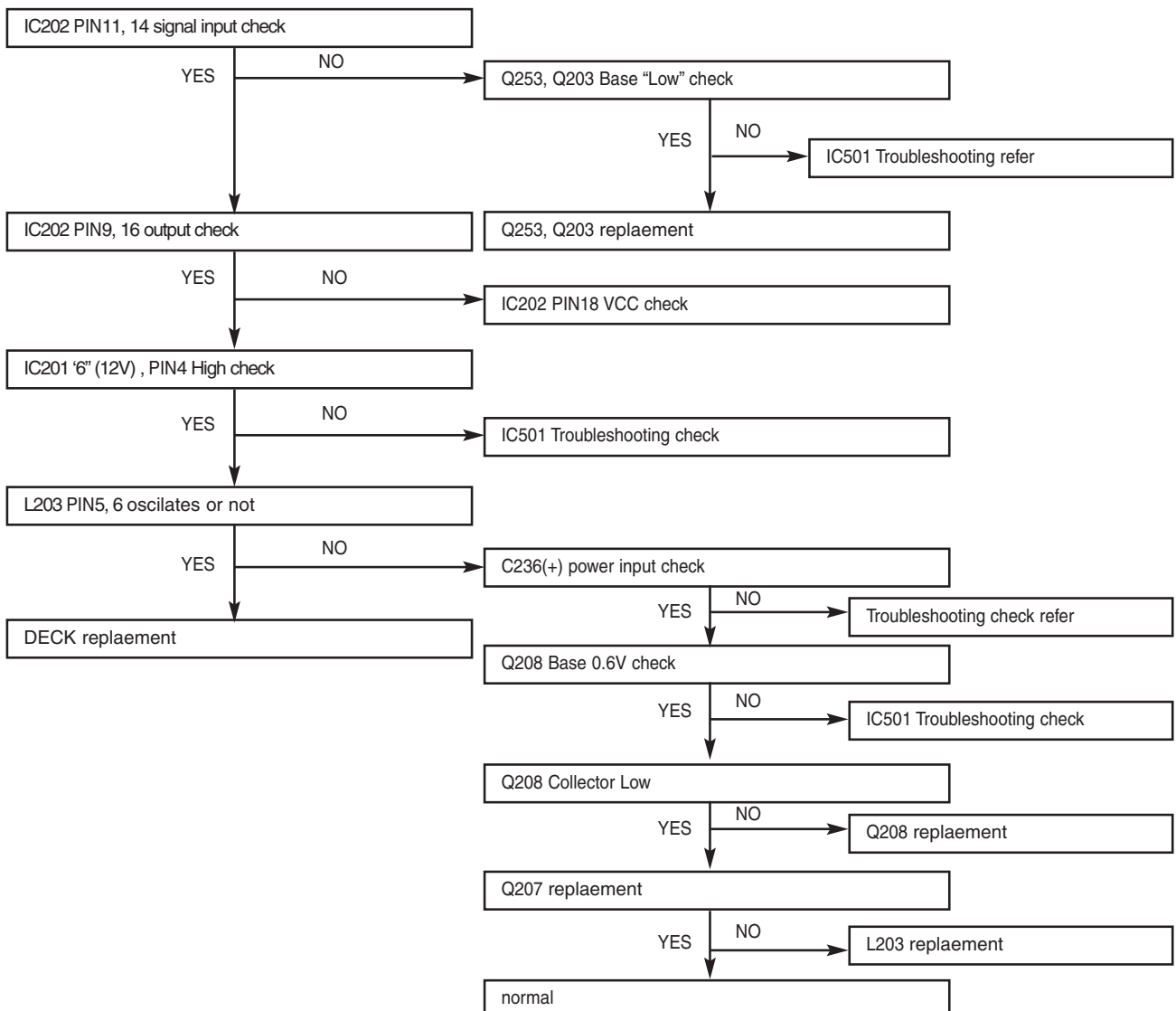
IC701(AMP IC) Troubleshooting



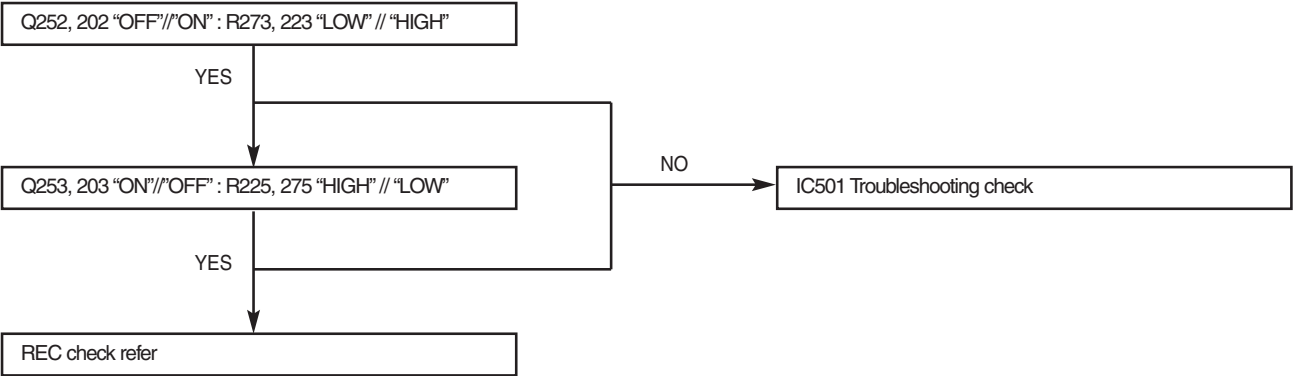
TAPE PLAY



TAPE REC check (Q252, Q202 On: R273, R223 High)

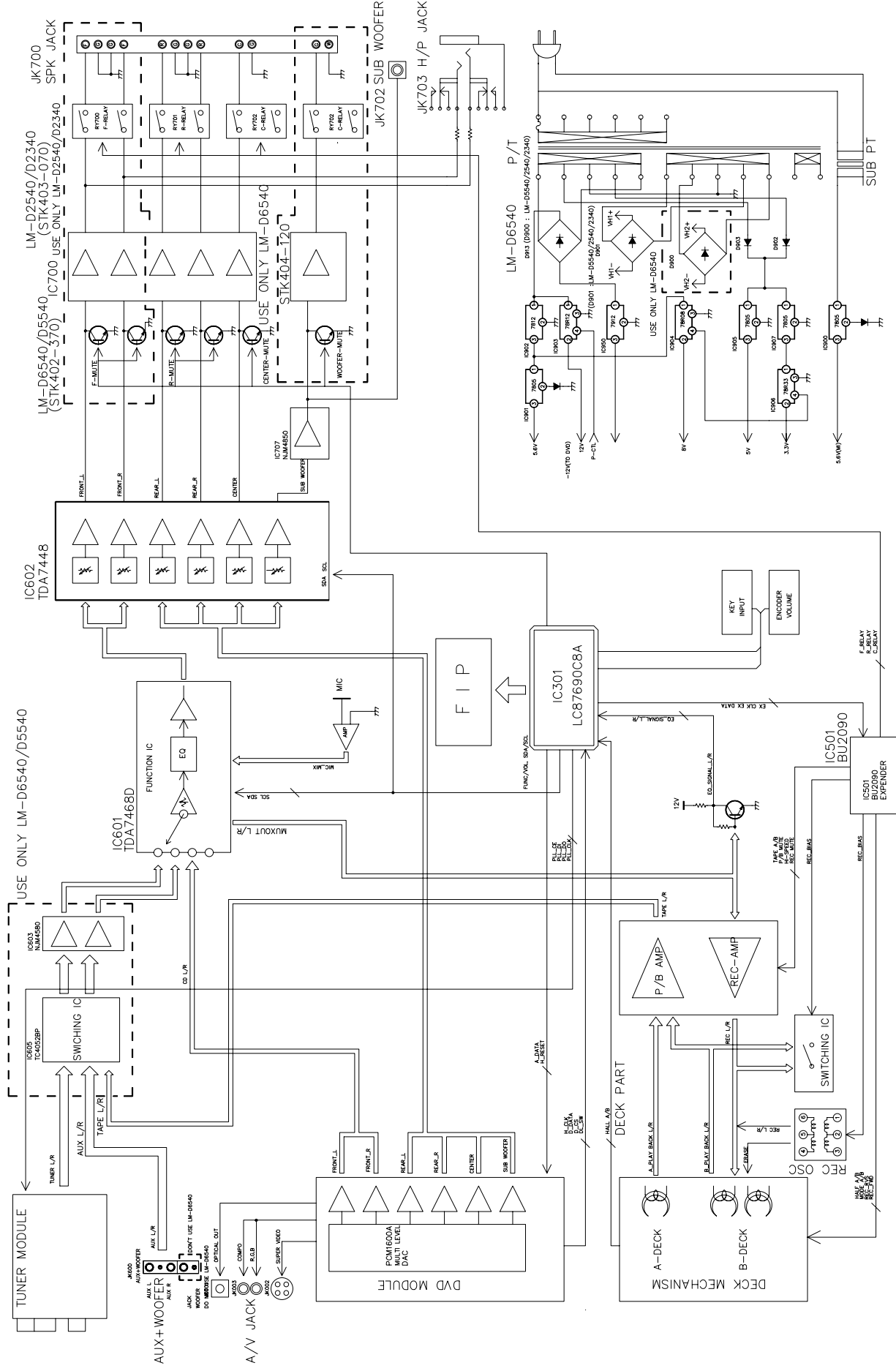


Dubbing check (“NORMAL”or “HIGH”) check



MEMO

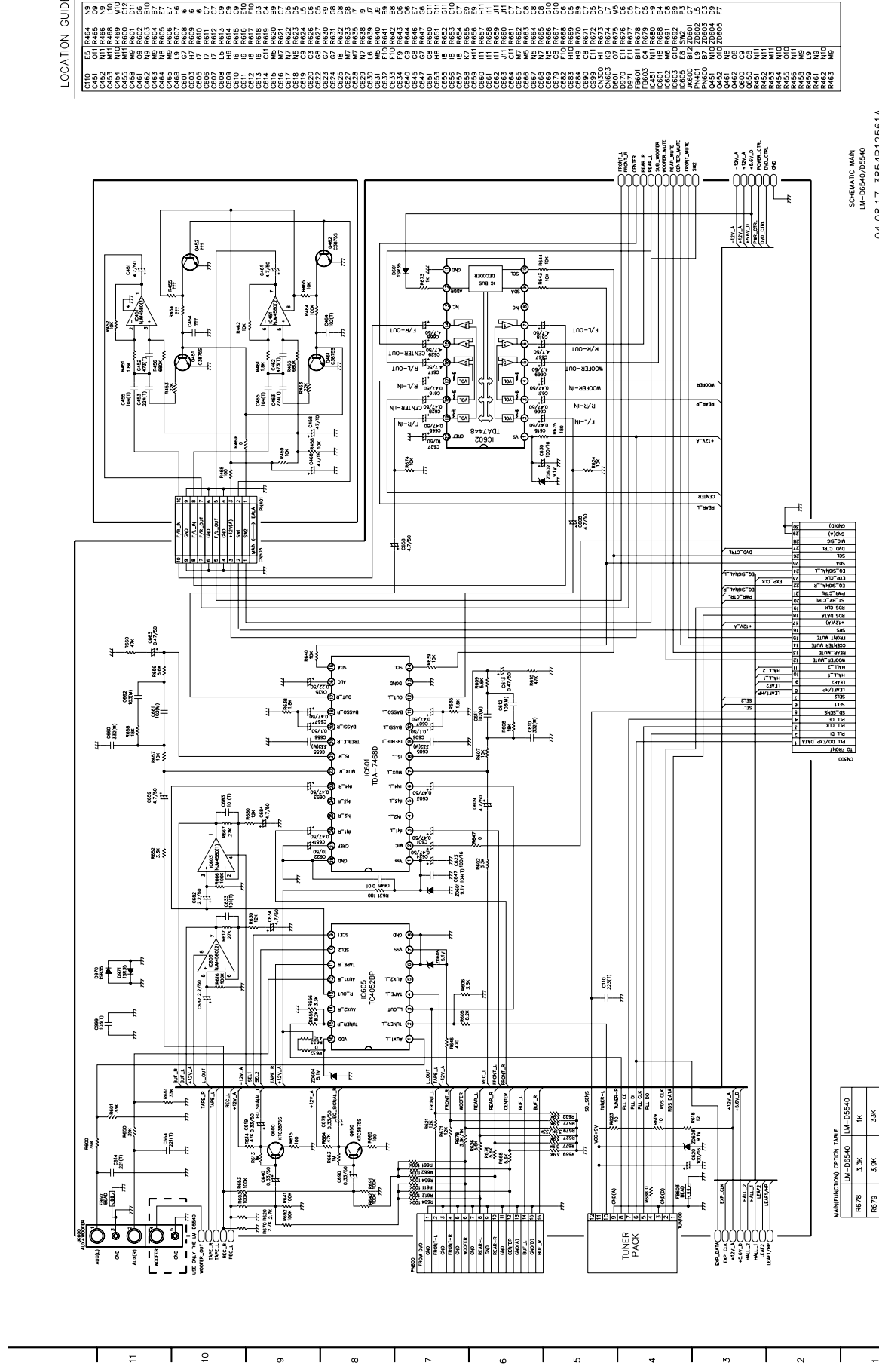
□ BLOCK DIAGRAM



BLOCK DIAGRAM
LM-D6540/D5540/D2340
3854R12568A

SCHEMATIC DIAGRAMS

- MAIN, OAO SCHEMATIC DIAGRAM



MAIN(FUNCTION) OPTION TABLE		
	LM-D6540	LM-D5540
R678	3.3K	1K
R679	3.9K	33K

LM-D6540/D5540
SCHEMATIC MAIN

04.08.17 3854R12561A

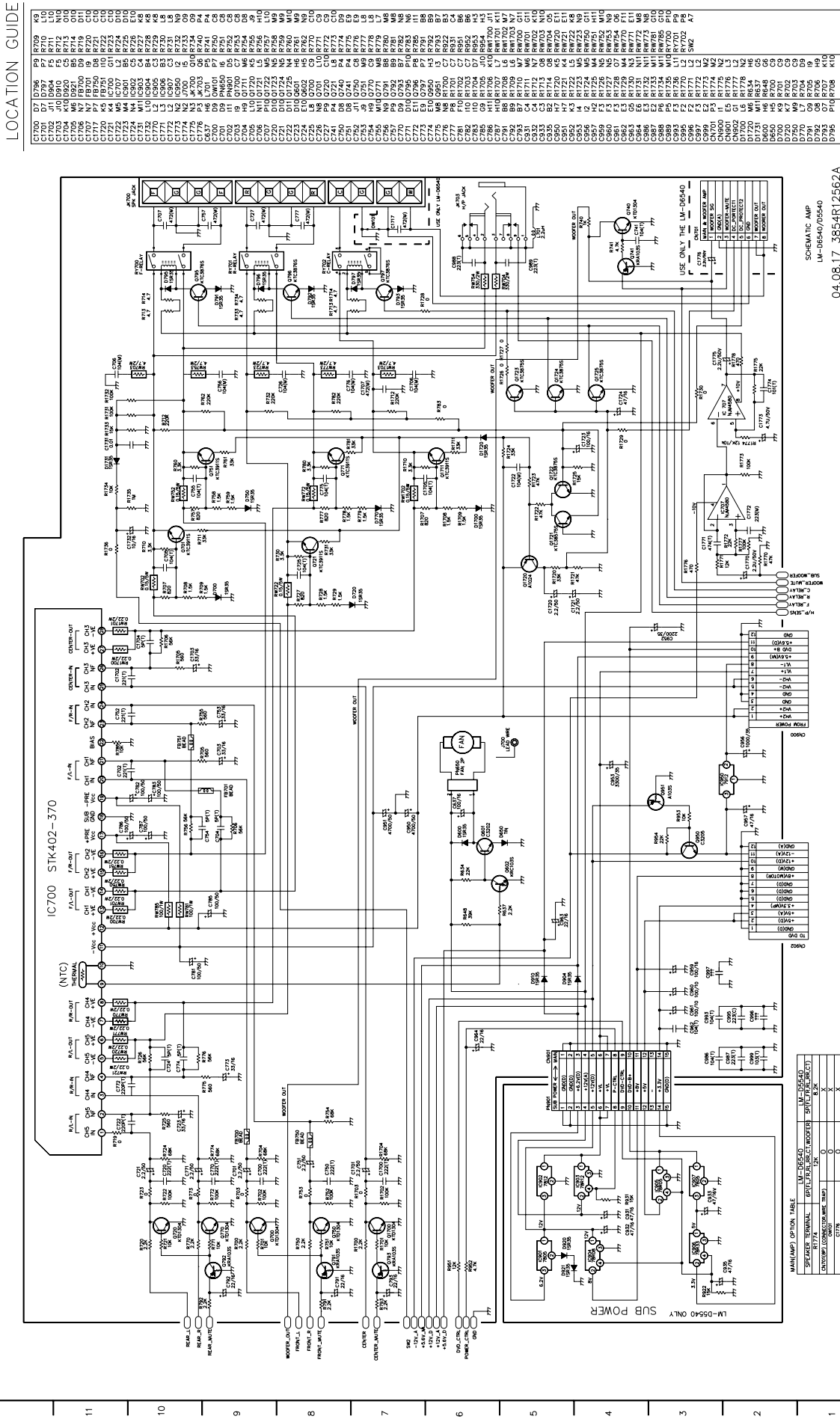
Timeline of the 2015-2016 season:

- 2-15: April, May, June
- 2-16: July, August, September, October, November, December, January, February, March

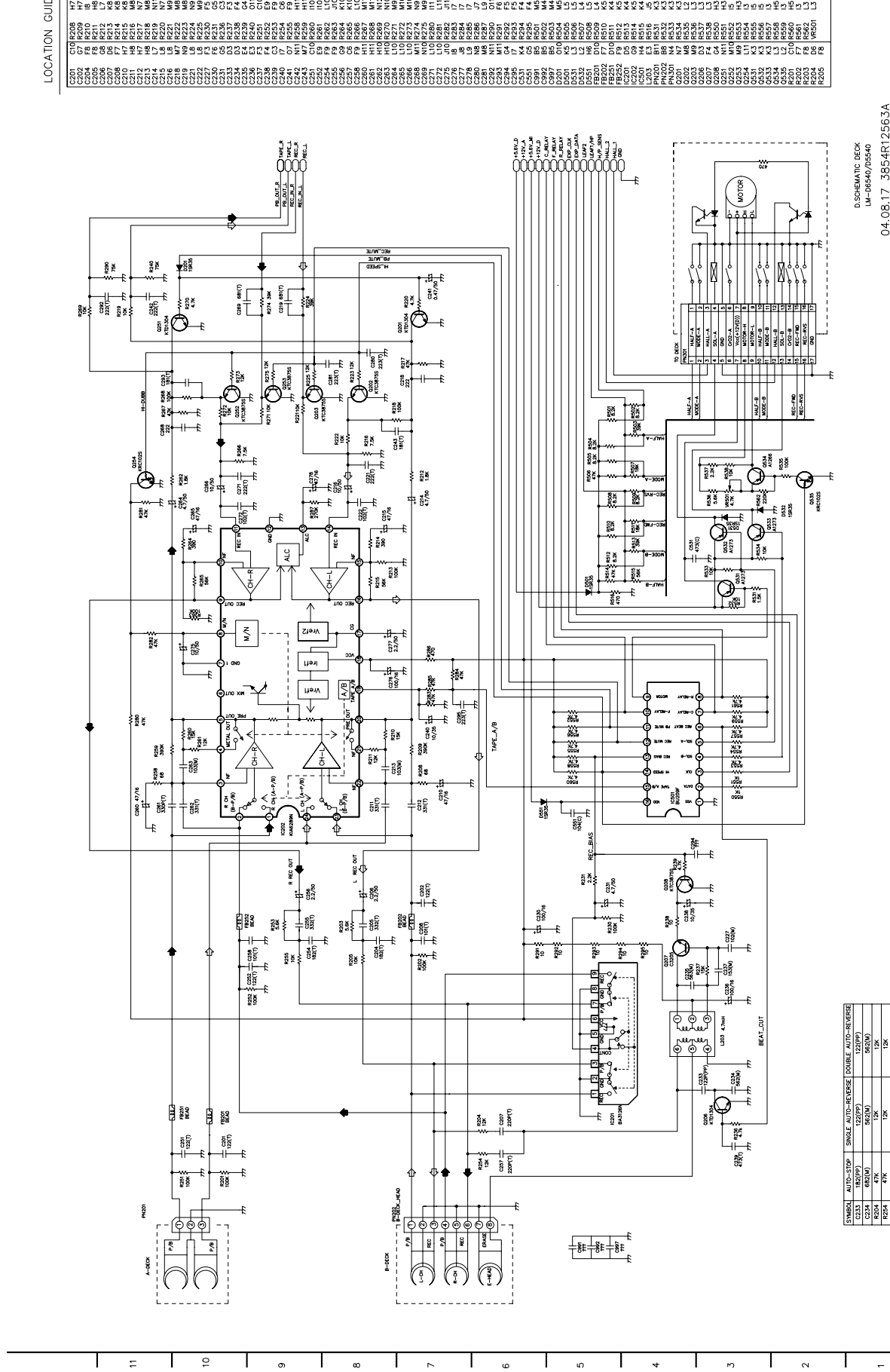
LOCATION GUIDE

C110	C5	R444	N9
C452	N1	R446	N9
C453	N1	R446	N9
C454	N1	R446	N9
C455	M1	R602	C12
C456	M1	R602	C12
C457	M1	R602	C12
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C718	M1	R602	C12
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C722	M1	R602	C12
C723	M1	R602	C12
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C734	M1	R602	C12
C735	M1	R602	C12
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C818	M1	R602	C12
C819	M1	R602	C12
C820	M1	R602	C12
C821	M1	R602	C12
C822	M1	R602	C12
C823	M1	R602	C12
C824	M1	R602	C12
C825	M1	R602	C12
C826			

• MAIN(AMP), SUB POWER SCHEMATIC DIAGRAM



• MAIN(DECK) SCHEMATIC DIAGRAM



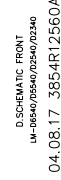
LOCATION GUIDE

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C202	G7	R209	H7
C203	F8	R211	H8
C204	D8	R212	H8
C205	D8	R213	H8
C206	F7	R214	H8
C207	H8	R215	H8
C208	F7	R216	H8
C209	H8	R217	H8
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LOCATION GUIDE

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LOCATION GUIDE

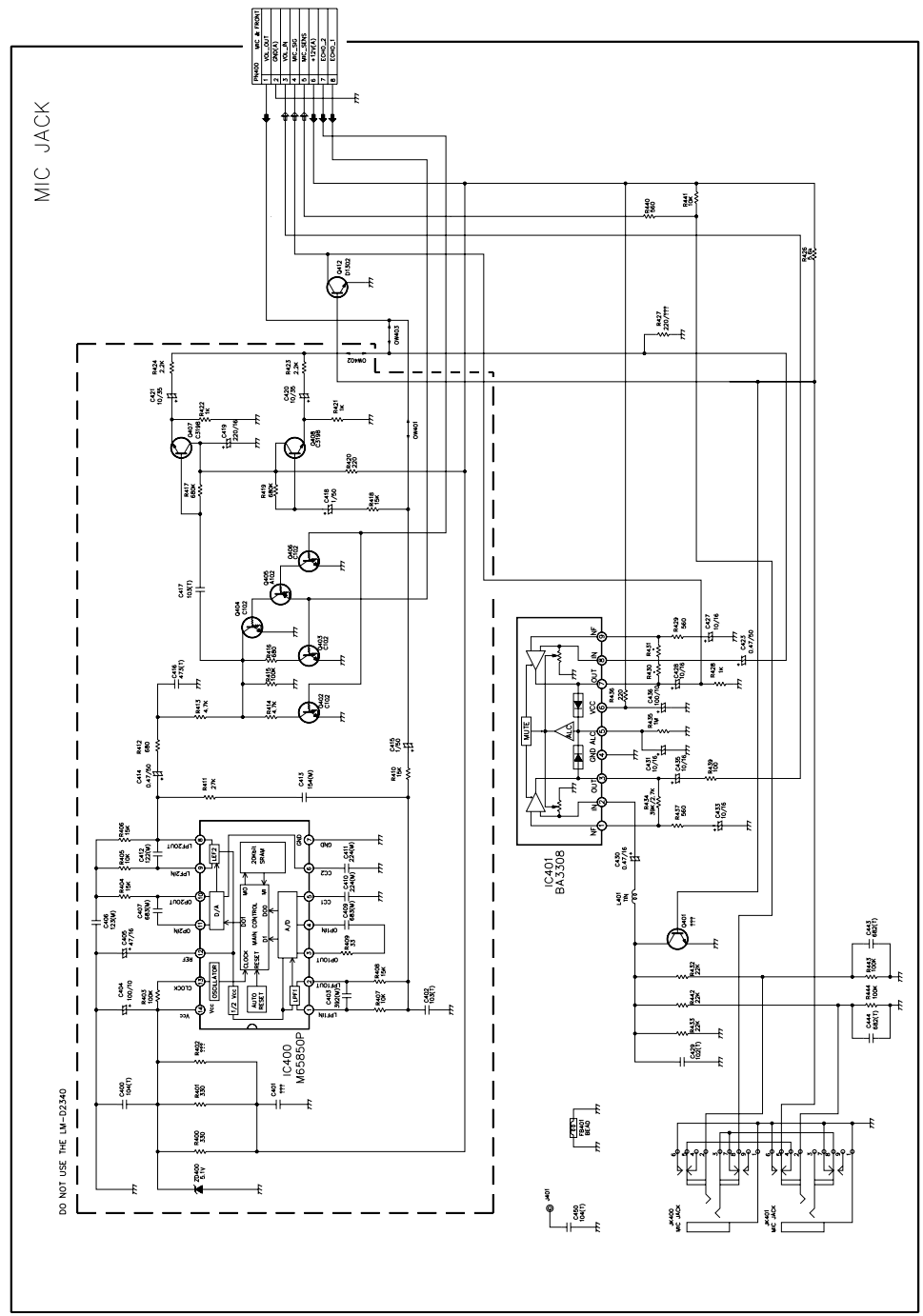


LM-D0540/00540/02540	LM-D2540
LD301 LD302 LD303 LD304 LD305 LD306 LD307 LD308 LD309 LD310 LD311 LD312 LD313 LD314 LD315 LD316 LD346 CS47	O (BLUE) X (???) 470

• MIC SCHEMATIC DIAGRAM

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C402	F8
C403	F10
C404	F10
C405	F10
C406	F10
C407	G9
C408	G9
C409	G9
C410	G8
C411	G10
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C431	G5
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C440	H4
C441	H4
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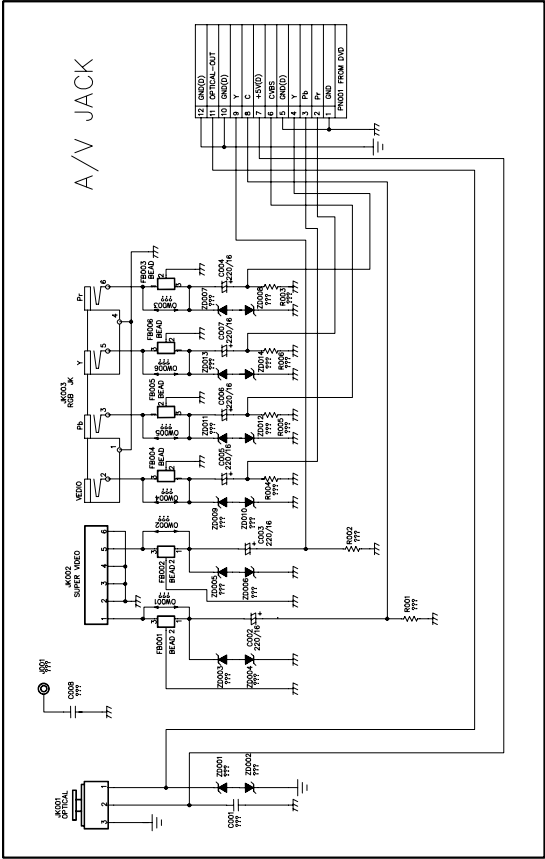
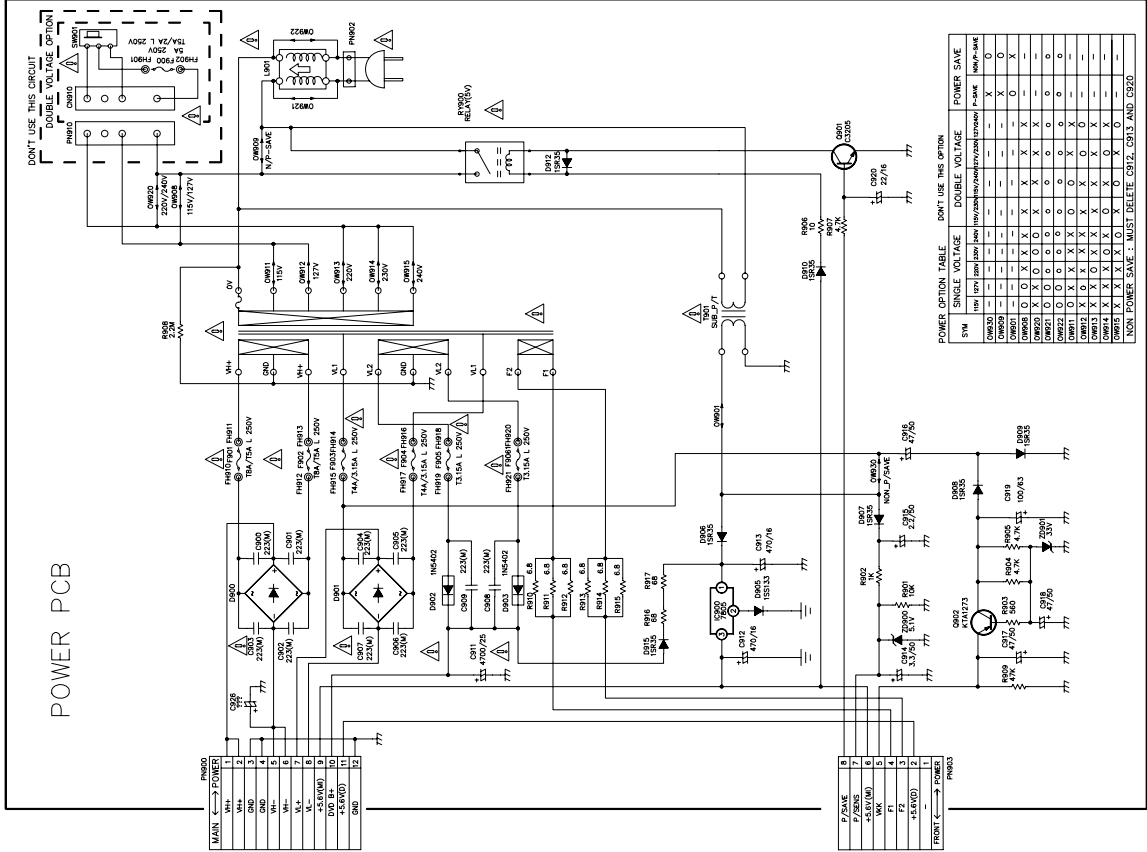


MIC OPTION TABLE (1)		MIC OPTION TABLE (2)	
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R402	10K	R402	10K
R403	10K	R403	10K
R404	10K	R404	10K
R405	10K	R405	10K
R406	10K	R406	10K
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R445	10K	R445	10K
R446	10K	R446	10K
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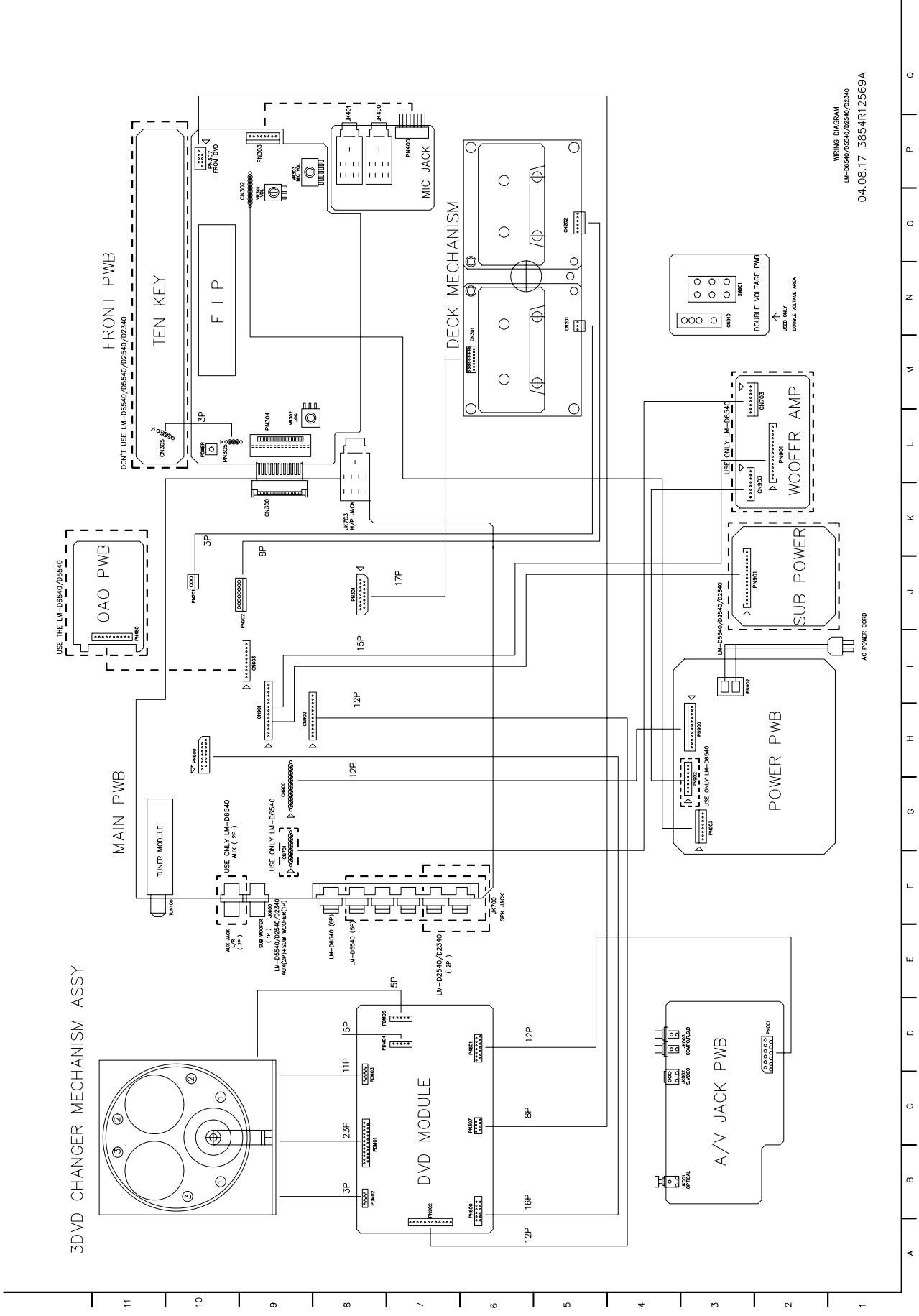
SCHEMATIC MIC
LM-D2340/D2340/D2340/D2340

04.08.17 3854R12565A

• POWER, A/V JACK SCHEMATIC DIAGRAM



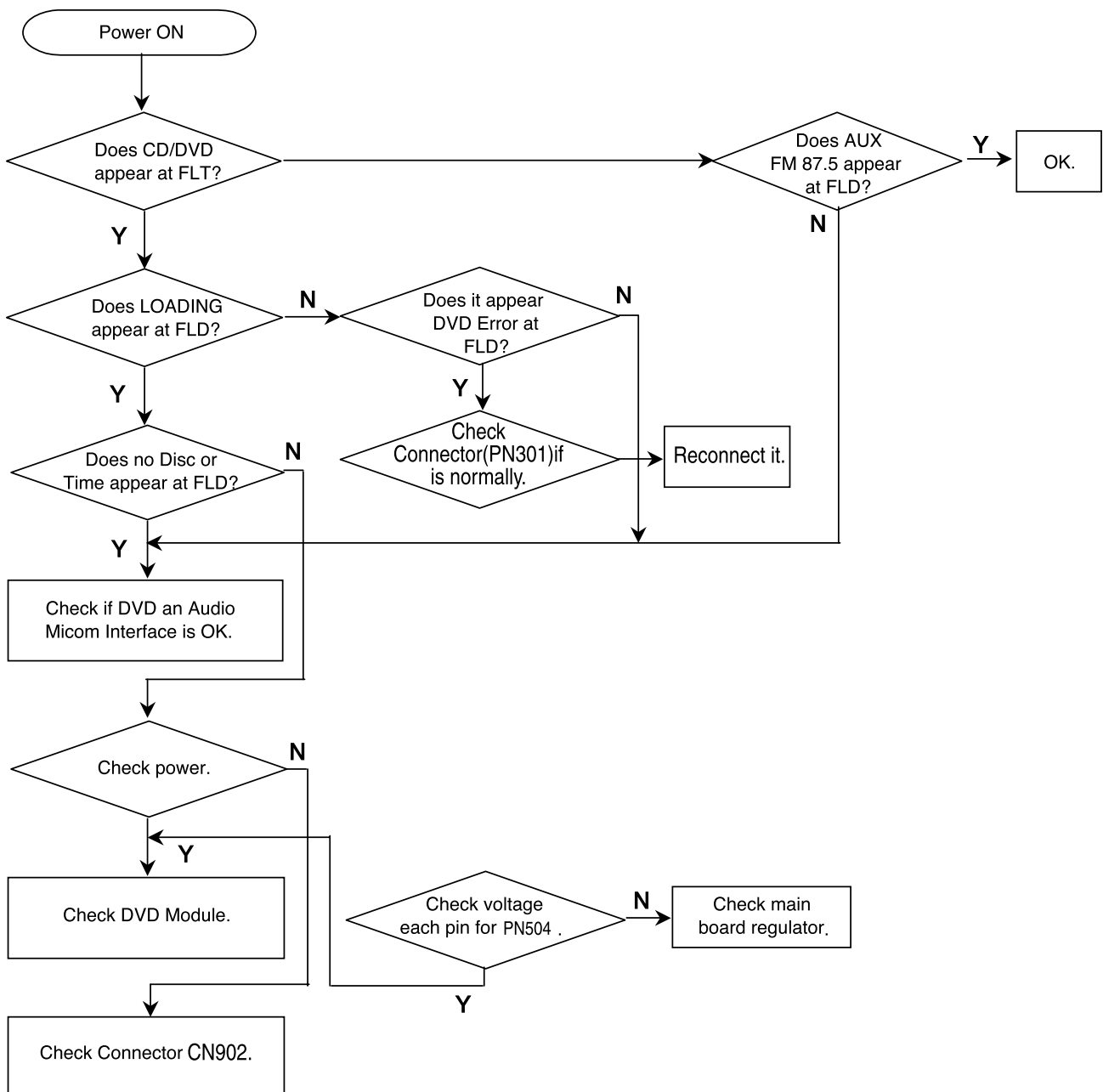
❑ WIRING DIAGRAM



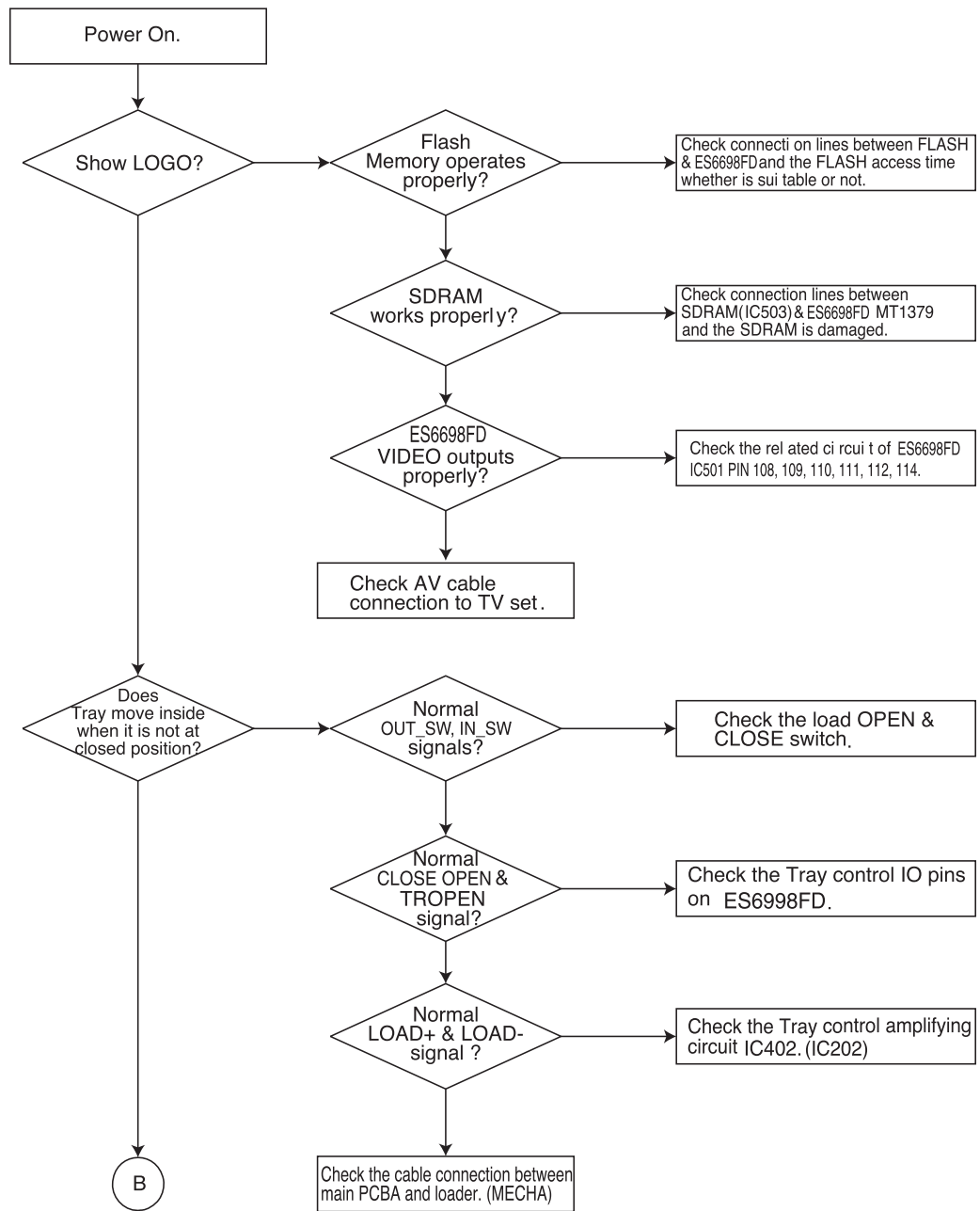
SECTION 3. DVD PART

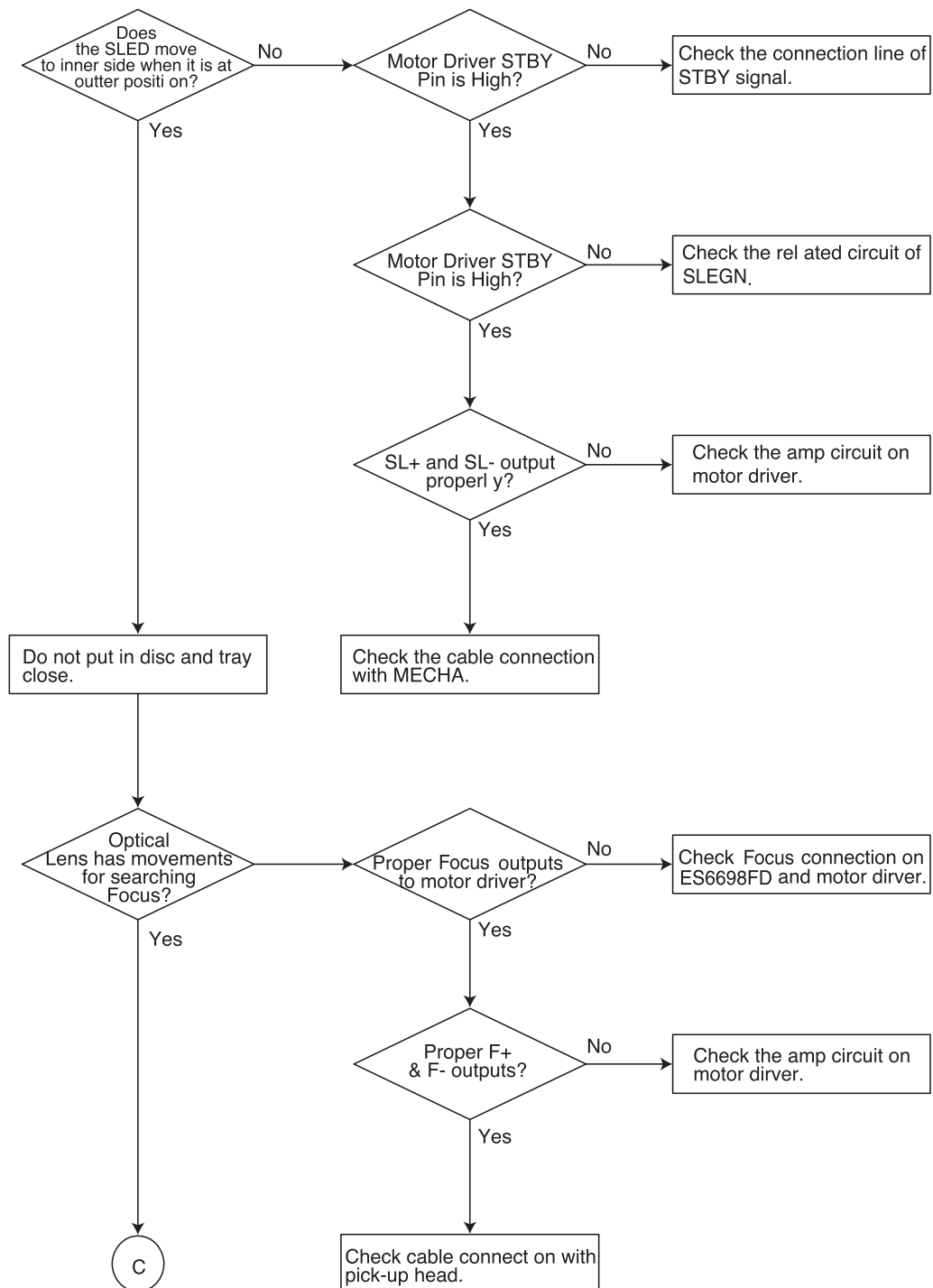
□ DVD ELECTRICAL TROUBLESHOOTING GUIDE

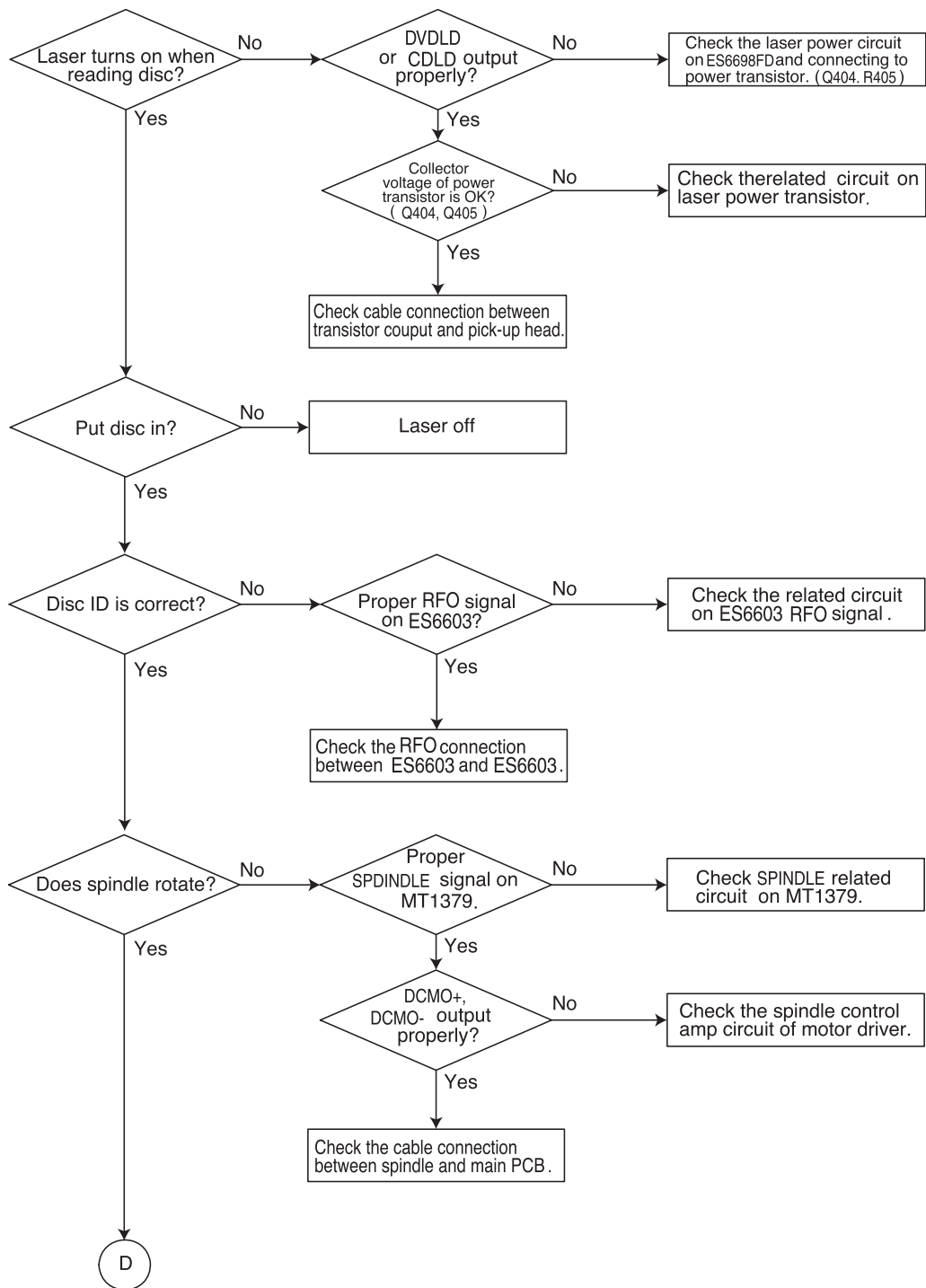
1. Power check flow

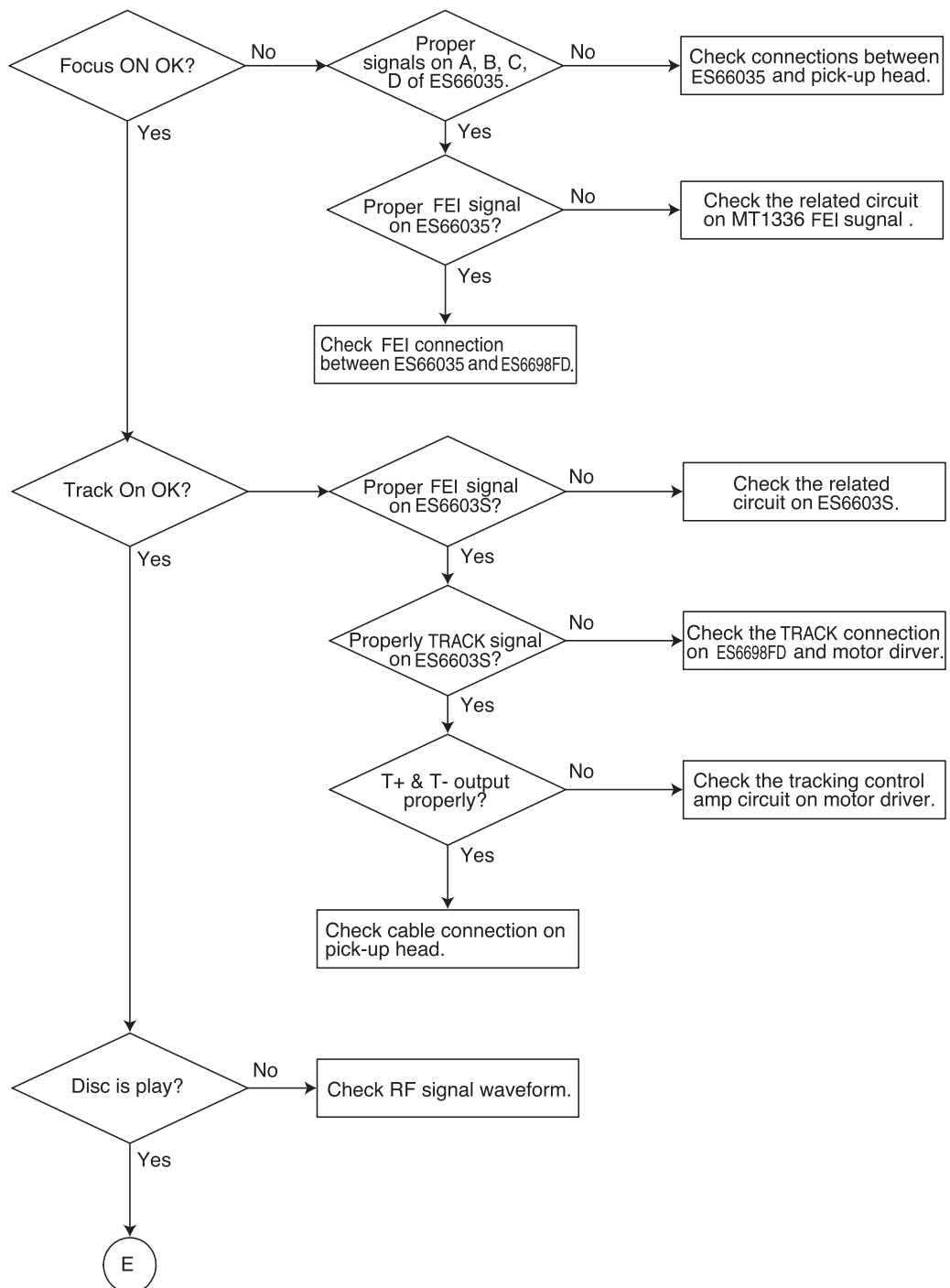


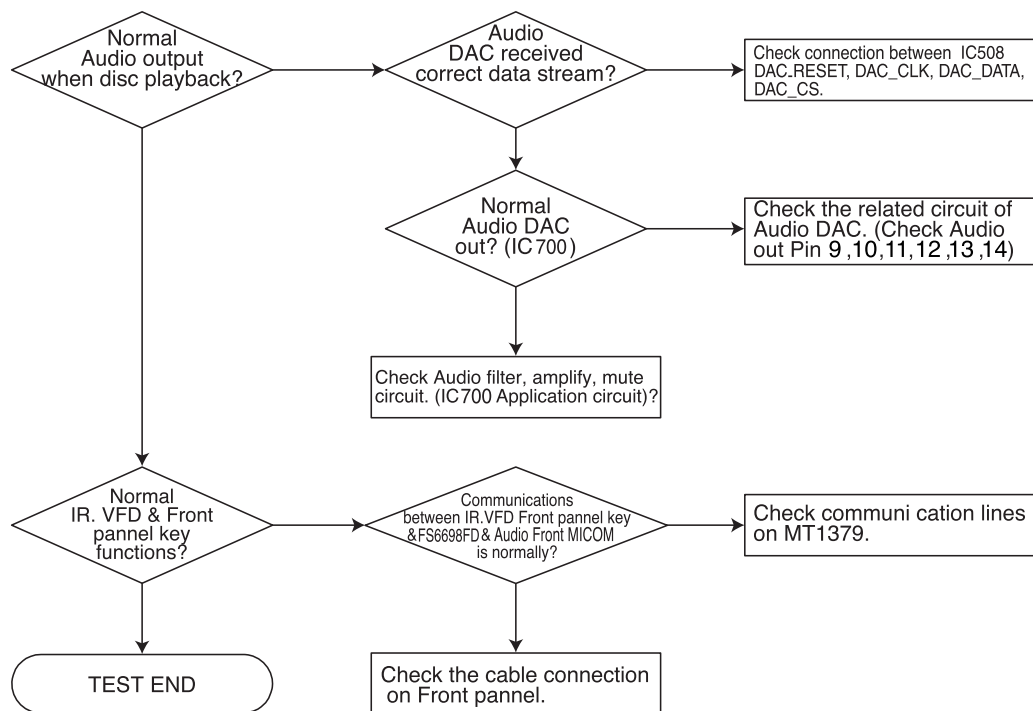
2. Test & debug flow







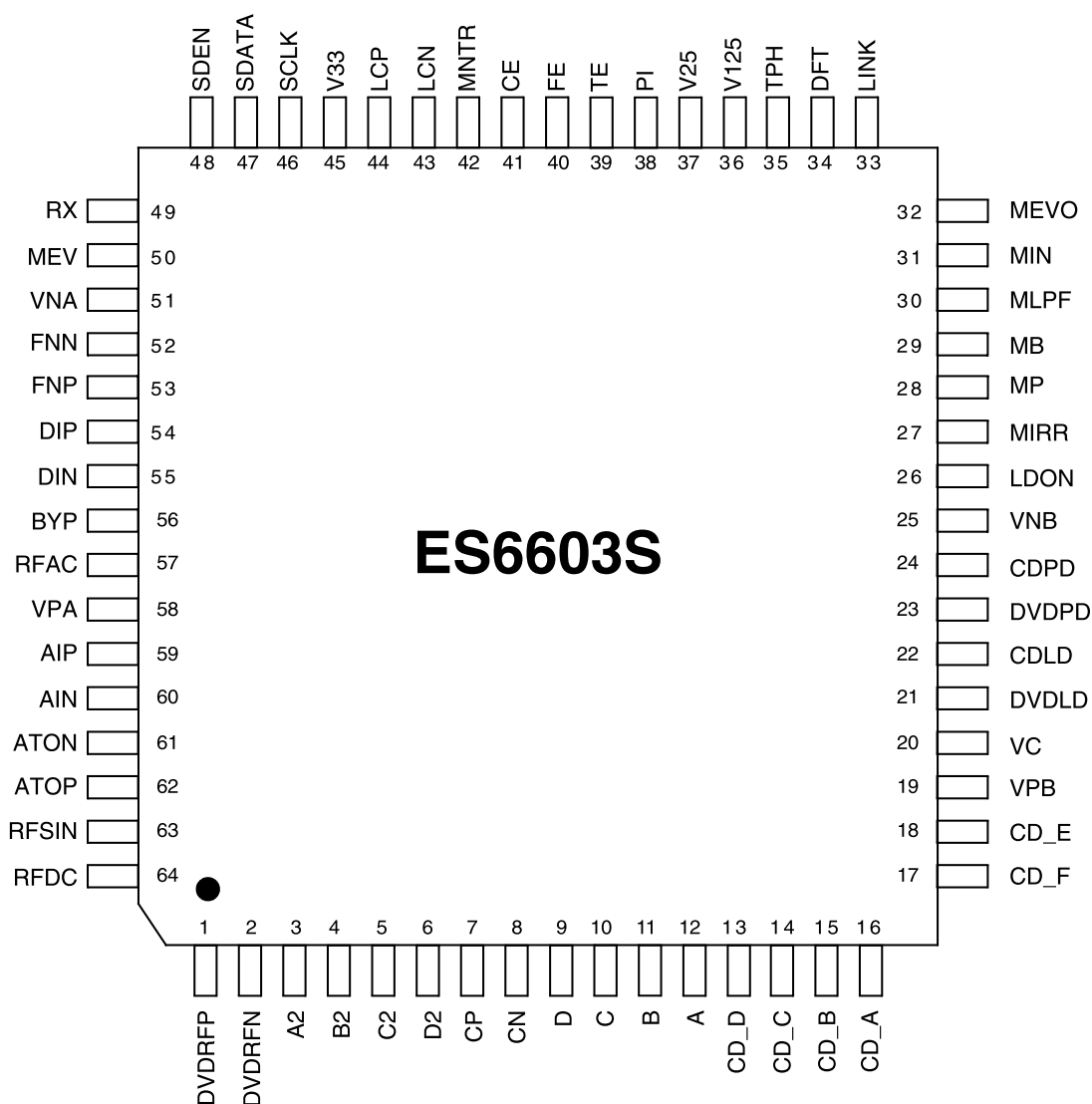




□ INTERNAL BLOCK DIAGRAM of ICs

• ES6603 (IC401) BLOCK DIAGRAM

Figure 1 depicts the ES6603 device pinout. The pound symbol (#) indicates an active-low signal.



ES6603 PIN DESCRIPTION

Table 1 lists the pin descriptions for the ES6603. The pound symbol (#) indicates an active-low signal.

Table 1 ES6603 Pin Descriptions List

Name	Pin Numbers	I/O	Definition
DVDRFP, DVDRFN	1, 2	I	Differential RF signal attenuator inputs.
A2, B2, C2, D2	3:6	I	AC coupled photo detector interface inputs for the differential phase detector (DPD) from the main beam photo matrix.
CP, CN	7, 8	—	Differential phase tracking low-pass filter pins. Connect CP to CN via capacitors.
D, C, B, A	9:12	I	Photo detector interface inputs from the main beam photo matrix.
CD_D, CD_C, CD_B, CD_A	13:16	I	CD photo detector interface inputs from the main beam photo matrix.
CD_F, CD_E	17, 18	I	CD photo detector interface inputs from the CD side beam photo detector; used for CD tracking detection.
VPB	19	P	Servo block power supply.
VC	20	O	Reference voltage out (VPB/2). Output impedance is less than 50Ω.
DVDLD	21	O	DVD APC output; controls laser power for DVD.
CDLD	22	O	CD APC output; controls laser power for CD.
DVDPD	23	I	DVD APC input.
CDPD	24	I	CD APC input.
VNB	25	G	Servo block ground.
LDON	26	I	APC On/Off control. A high level activates LD output. (open is low)
MIRR	27	O	Mirror detect output.
MP, MB	28, 29	I	Mirror top and bottom hold pins. Connected to VPB pin 19 via capacitors.
MLPF	30	I	Mirror low-pass filter pins. Connected to VPB pin 19 via a capacitor.
MIN	31	I	RF input signal for mirror. AC coupled inputs for the mirror detection circuit from MEVO pin 32.
MEVO	32	O	RFDC bottom envelope out. Pull-In or bottom clamped RF envelope signal output for mirror detection.
LINK	33	I,O	Linking Signal In/Mirror Monitor Out. In the linking area, the mirror and tracking error outputs are disabled when this pin goes high. When the monitor output signal is selected by the Control H register, mirror-related signals can be observed.
DFT	34	O	Defect output. When the Pull-In signal level is below the detection level, or when the RF signal level is below the detection level, the DFT output goes high. The defect output is selected by the serial port.
TPH	35	I	Pull-In top hold. Connected to VPB pin 19 via a capacitor.
V125	36	O	1.25V servo block reference voltage output.
V25	37	P	2.5V servo output reference power supply.
PI	38	O	Pull-In signal out. The summing signal output of A, B, C, D, or CD_A, CD_B, CD_C, or CD_D. Reference to V25/3.
TE	39	O	Tracking error output reference to V125 pin 36.
FE	40	O	Focusing error output reference to V125 pin 36.

Table 1 ES6603 Pin Descriptions List (Continued)

Name	Pin Numbers	I/O	Definition
CE	41	O	Center error output reference to V125 pin 36.
MNTR	42	O	Monitor out signal. Output is selectable by register settings.
LCN, LCP	43, 44	I	Lens shift offset cancellation low-pass filter pins. Connect LCN to LCP via a capacitor.
V33	4 5	P	3.3V output buffers power supply.
SCLK	46	I	Serial clock from ES66x8.
SDATA	47	I/O	Serial data I/O.
SDEN	48	I	Serial data enable. Enabled by an active-high signal.
RX	49	I	Reference resistor. Connected to ground via a 12.0k Ω , 1% resistor..
MEV	50	I	RFDC bottom envelope. Connected to VPA pin 58 via a capacitor.
VNA	51	G	RF block and serial port ground.
FNN, FNP	52, 53	O	Differential outputs of equalizer/filter.
DIP, DIN	54, 55	I	Differential analog inputs to the RF single-end output buffer and full wave rectifier.
BYP	56	I	AGC amplifier gain bypass. Tied to VPA via a capacitor.
RFAC	57	O	Single-ended RF output.
VPA	58	P	RF block and serial port power supply.
AIP, AIN	59, 60	I	Differential AGC amplifier inputs.
ATON, ATOP	61, 62	O	Differential attenuator outputs.
RFSIN	63	I	Single-ended RF signal attenuator input.
RFDC	64	O	Single-ended RF summing output.

ES6603 DEVICE INTERFACES

Table 2 lists the device interfaces for the ES6603

Table 2 ES6603 Device Interfaces

Name	Pin Numbers	I/O	Definition
AGC Interface	59, 60	I	Differential AGC amplifier inputs [AIP] and [AIN].
Automatic Laser Power Control (APC) Interface	21	O	APC laser power control for DVD [DVDLD].
	22	O	APC laser power control for CD [CDLD].
	23	I	APC photo diode in for DVD [DVDPD].
	24	I	APC photo diode in for CD [CDPD].
	26	I	APC input on/off control [LDON].
CD/DVD Photo Detector Interface	3:6		DVD differential phase detector matrix inputs [A2], [B2], [C2], and [D2].
	9:12	I	DVD single-ended phase detector matrix inputs [A], [B], [C], and [D].
	13:16	I	CD photo detector interface inputs [CD_A], [CD_B], [CD_C] and [CD_D].
	17, 18	I	CD side beam photo detector tracking outputs [CD_E] and [CD_F].
Embedded Servo DSP Interface	26	I	APC input on/off control [LDON] from embedded servo DSP.
	33	I/O	Linking signal and mirror monitor control I/O [LINK].
	34	O	Defect output [DFT] to embedded servo DSP.
	38	O	Pull-In signal [PI] to embedded servo DSP.
	39	O	Tracking error [TE] to embedded servo DSP.
	40	O	Focusing error [FE] to embedded servo DSP.
	41	O	Center error [CE] to embedded servo DSP.
	46	I	Serial clock [SCLK] from embedded servo DSP.
	47	I/O	Serial data I/O [SDATA] for embedded servo DSP.
	48	I	Serial data enable [SDEN] from embedded servo DSP.
Filtering and Reference Voltage	7, 8	I	Differential phase tracking low-pass filters [CP] and [CN].
	20	O	DC bias reference voltage [VC].
	30	I	Mirror low-pass filter [MLPF].
	36	O	Servo block reference voltage [V125].
	43, 44	I	Lens shift offset cancellation low-pass filters [LCP] and [LCN].
	64	O	Single-ended RF summing output reference [RFDC].
Power and Ground	19	P	Servo block port power supply [VPB].
	25	G	Servo block ground [VNB].
	37	P	2.5V reference voltage servo output power supply [V25].
	45	P	3.3V output buffers power supply [V33].
	51	G	RF block and serial port ground [VNA].
	58	P	RF block and serial port power supply [VPA].
AGC and Filter Interface	1,2	I	Differential RF signal attenuator inputs [DVDRFP] and [DVDRFN].
	52, 53	O	Differential normal filter outputs [FNP] and [FNN].
	54, 55	I	Differential analog RF buffer inputs [DIP] and [DIN].
	57	O	Single-ended RF output [RFAC].
	63	I	Single-ended RF signal attenuator input [RFSIN].
	61, 62	O	Differential attenuator outputs [ATOP] and [ATON].
Serial Port Interface	46	I	Serial clock from ES66x8 [SCLK].
	47	I/O	Serial data I/O [SDATA].
	48	I	Serial data enable [SDEN].

• BA5954FM (IC404)
BLOCK DIAGRAM

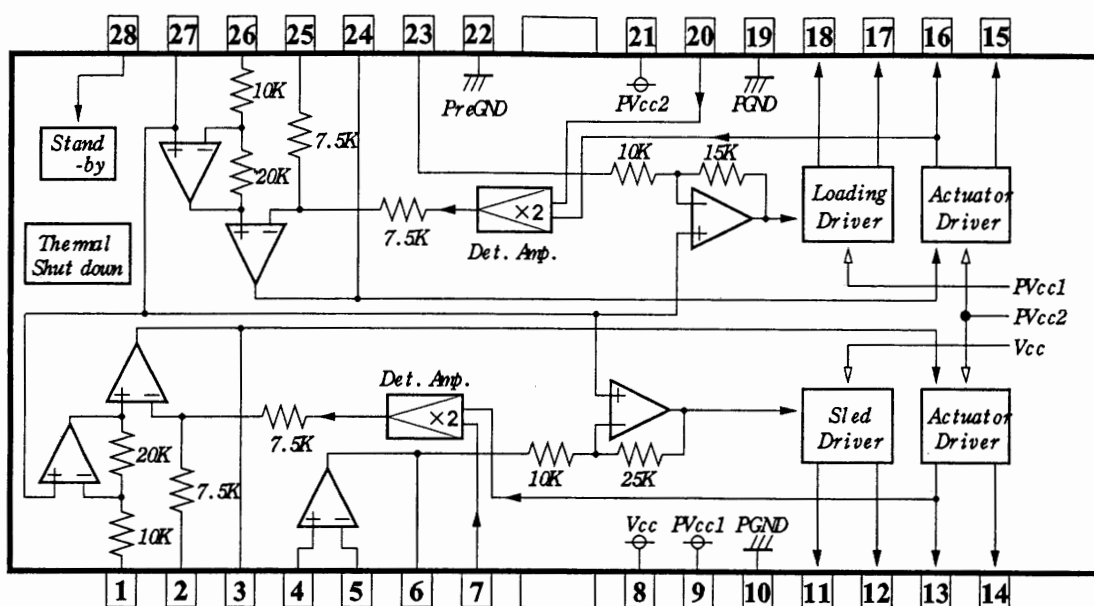
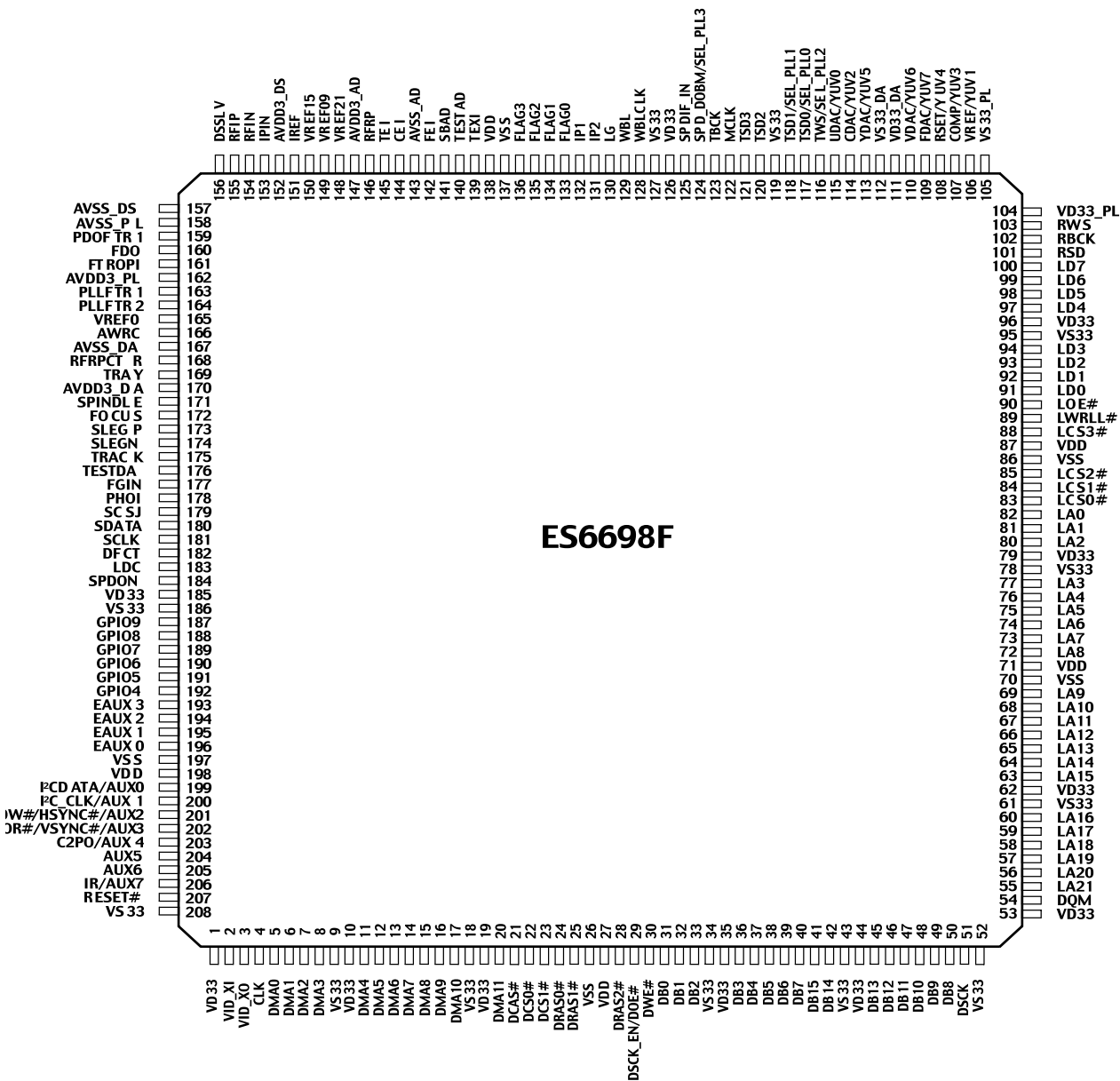


Figure 3

Pin description

No	Symbol	Function	No	Symbol	Function
1	VINFC	Input for focus driver	15	VOTK+	Non inverted output of tracking
2	CFCerr1	Connection with capacitor for error amplifier	16	VOTK-	Inverted output of tracking
3	CFCerr2		17	VOLD+	Non inverted output of loading
4	VINSL+	Non inverting Input for OP- amp	18	VOLD-	Inverted output of loading
5	VINSL-	Inverting input for OP- amp	19	PGND	GND for power block
6	VO SL	Output of OP- amp	20	VNFTK	Feedback for tracking driver
7	VNFFC	Feedback for focus driver	21	PVcc2	Vcc for power block of actuator
8	Vcc	Vcc for pre- drive block and power block of sled	22	PreGND	GND for pre- drive block
9	PVcc1	Vcc for power block of loading	23	VINLD	Input for loading driver
10	PGND	GND for power block	24	CTKerr2	Connection with capacitor for error amplifier
11	VO SL-	Inverted output of sled	25	CTKerr1	
12	VO SL+	Non inverted output of sled	26	VINTK	Input for tracking driver
13	VO FC-	Inverted output of focus	27	BIAS	Input for reference voltage
14	VO FC+	Non inverted output of focus	28	STBY	Input for stand-by control

- **ES6698 (IC501)**
BLOCK DIAGRAM



ES6698 PIN DESCRIPTION

Table 1 lists the pin descriptions for the ES6698.

Table 1 ES6698 Pin Description

Names	Pin Numbers	I/O	Definitions
VD33	1, 10, 19, 35, 44, 53, 62, 79, 96, 126, 185	P	I/O power supply.
VID_XI	2	I	Crystal input.
VID_XO	3	O	Crystal output.
CLK	4	I	System clock.
DMA[11:0]	5:8 11:17, 20	O	DRAM address bus.
VS33	9, 18, 34, 43, 52, 61, 78, 95, 119, 127, 186, 208	G	Ground for I/O power supply.
DCAS#	21	O	DRAM column address strobe (active-low).
DCS[1:0]#	22, 23	O	DRAM chip select (active-low).
DRAS[2:0]#	24, 25, 28	O	DRAM row address strobe (active-low).
VSS	26, 70, 86, 137, 197	G	Ground for core power supply.
VDD	27, 71, 87, 138, 198	P	Core power supply.
DSCK_EN	29	O	DRAM clock enable output.
DOE#		O	DRAM output enable (active-low).
DWE#	30	O	DRAM write enable (active-low).
DB[15:0]	31:33, 36:42, 45:50	I/O	DRAM data bus.
DSCK	51	O	Output clock to DRAM.
DQM	54	O	Data input/output mask.
LA[21:0]	55:60, 63:69, 72:77, 80:82	O	RISC port address bus.
LCS[3:0]#	83:85, 88	O	RISC port chip select (active-low).
LWRL#	89	O	RISC port low-byte write enable (active-low).
LOE#	90	O	RISC port output enable (active-low).
LD[7:0]	91:94, 97:100	I/O	RISC port data bus; (5V tolerant input).
RSD	101	I	Audio receive serial data; (5V tolerant input).
RBCK	102	I	Audio receive bit clock; (5V tolerant input).
RWS	103	I	Audio receive frame sync; (5V tolerant input).
VD33_PL	104	P	Power for PLL blocks.
VS33_PL	105	G	Ground for PLL blocks.
VREF	106	I	Internal voltage reference to video DAC.
YUV1		O	YUV pixel 1 output data.
COMP	107	I	Compensation input.
YUV3		O	YUV pixel 3 output data.

Table 1 ES6698 Pin Description (Continued)

Names	Pin Numbers	I/O	Definitions																																																																																																						
RSET	108	I	DAC current adjustment resistor input.																																																																																																						
YUV4		O	YUV pixel 4 output data.																																																																																																						
FDAC	109	O	Video DAC output. Refer to description and matrix for UDAC pin 115.																																																																																																						
YUV7		O	YUV pixel 7 output data.																																																																																																						
VDAC	110	O	Video DAC output. Refer to description and matrix for UDAC pin 115.																																																																																																						
YUV6		O	YUV pixel 6 output data.																																																																																																						
VD33_DA	111	P	Power for I/O power supply for VDAC.																																																																																																						
VS33_DA	112	G	Ground for I/O power supply for VDAC.																																																																																																						
YDAC	113	O	Video DAC output. Refer to description and matrix for UDAC pin 115.																																																																																																						
YUV5		O	YUV pixel 5 output data.																																																																																																						
CDAC	114	O	Video DAC output. Refer to description and matrix for UDAC pin 115.																																																																																																						
YUV2		O	YUV pixel 2 output data.																																																																																																						
UDAC	115	O	Video DAC output. <table><tr><th>Pin</th><th>109</th><th>110</th><th>113</th><th>114</th><th>115</th></tr><tr><th>Value</th><th>F DAC</th><th>V DAC</th><th>Y DAC</th><th>C DAC</th><th>U DAC</th></tr><tr><td>0</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>C</td><td>N/A</td></tr><tr><td>1</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>C</td><td>CVBS2</td></tr><tr><td>2</td><td>CVBS/Chroma</td><td>N/A</td><td>Y</td><td>C</td><td>N/A</td></tr><tr><td>3</td><td>CVBS/Chroma</td><td>CVBS1</td><td>N/A</td><td>N/A</td><td>CVBS2</td></tr><tr><td>4</td><td>CVBS/Chroma</td><td>CVBS1</td><td>N/A</td><td>N/A</td><td>N/A</td></tr><tr><td>5</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>Pb</td><td>Pr</td></tr><tr><td>6</td><td>CVBS/Chroma</td><td>N/A</td><td>Y</td><td>Pb</td><td>Pr</td></tr><tr><td>7</td><td>N/A</td><td>SYNC</td><td>G</td><td>B</td><td>R</td></tr><tr><td>8</td><td>CVBS/Chroma</td><td>Chroma</td><td>Y</td><td>Pb</td><td>Pr</td></tr><tr><td>9</td><td>CVBS</td><td>CVBS1</td><td>G</td><td>B</td><td>R</td></tr><tr><td>10</td><td>CVBS</td><td>CVBS1</td><td>G</td><td>R</td><td>B</td></tr><tr><td>11</td><td>N/A</td><td>SYNC</td><td>G</td><td>R</td><td>B</td></tr><tr><td>12</td><td>CVBS/Chroma</td><td>N/A</td><td>Y</td><td>Pr</td><td>Pb</td></tr><tr><td>13</td><td>CVBS/Chroma</td><td>CVBS1</td><td>Y</td><td>Pr</td><td>Pb</td></tr><tr><td>14</td><td>Chroma</td><td>Y</td><td>G</td><td>R</td><td>B</td></tr></table> F: CVBS/chroma signal for simultaneous mode. Y: Luma component for YUV and Y/C processing. C: Chrominance signal for Y/C processing. U: Chrominance component signal for YUV mode. V: Chrominance component signal for YUV mode.	Pin	109	110	113	114	115	Value	F DAC	V DAC	Y DAC	C DAC	U DAC	0	CVBS/Chroma	CVBS1	Y	C	N/A	1	CVBS/Chroma	CVBS1	Y	C	CVBS2	2	CVBS/Chroma	N/A	Y	C	N/A	3	CVBS/Chroma	CVBS1	N/A	N/A	CVBS2	4	CVBS/Chroma	CVBS1	N/A	N/A	N/A	5	CVBS/Chroma	CVBS1	Y	Pb	Pr	6	CVBS/Chroma	N/A	Y	Pb	Pr	7	N/A	SYNC	G	B	R	8	CVBS/Chroma	Chroma	Y	Pb	Pr	9	CVBS	CVBS1	G	B	R	10	CVBS	CVBS1	G	R	B	11	N/A	SYNC	G	R	B	12	CVBS/Chroma	N/A	Y	Pr	Pb	13	CVBS/Chroma	CVBS1	Y	Pr	Pb	14	Chroma	Y	G	R	B
Pin		109	110	113	114	115																																																																																																			
Value		F DAC	V DAC	Y DAC	C DAC	U DAC																																																																																																			
0		CVBS/Chroma	CVBS1	Y	C	N/A																																																																																																			
1		CVBS/Chroma	CVBS1	Y	C	CVBS2																																																																																																			
2		CVBS/Chroma	N/A	Y	C	N/A																																																																																																			
3		CVBS/Chroma	CVBS1	N/A	N/A	CVBS2																																																																																																			
4		CVBS/Chroma	CVBS1	N/A	N/A	N/A																																																																																																			
5		CVBS/Chroma	CVBS1	Y	Pb	Pr																																																																																																			
6		CVBS/Chroma	N/A	Y	Pb	Pr																																																																																																			
7		N/A	SYNC	G	B	R																																																																																																			
8		CVBS/Chroma	Chroma	Y	Pb	Pr																																																																																																			
9		CVBS	CVBS1	G	B	R																																																																																																			
10		CVBS	CVBS1	G	R	B																																																																																																			
11		N/A	SYNC	G	R	B																																																																																																			
12		CVBS/Chroma	N/A	Y	Pr	Pb																																																																																																			
13		CVBS/Chroma	CVBS1	Y	Pr	Pb																																																																																																			
14		Chroma	Y	G	R	B																																																																																																			
YUV0		O	YUV pixel 0 output data.																																																																																																						

Table 1 ES6698 Pin Description (Continued)

Names	Pin Numbers	I/O	Definitions																																				
TWS	116 I	O	Audio transmit frame sync output.																																				
SEL_PLL2			System and DSCK output clock frequency selection is made at the rising edge of RESET#. The matrix below lists the available clock frequencies and their respective PLL bit settings. Strapped to VCC or ground via 4.7-kΩ resistor; read-only during reset. <table><tr><th>SEL_PLL 2</th><th>SEL_PLL1</th><th>SEL_PLL0</th><th>Clock Type (MHz)</th></tr><tr><td>0</td><td>0</td><td>0</td><td>CLK X 4.5</td></tr><tr><td>0</td><td>0</td><td>1</td><td>CLK X 5.0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Bypass</td></tr><tr><td>0</td><td>1</td><td>1</td><td>CLK X 4.0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>CLK X 4.25</td></tr><tr><td>1</td><td>0</td><td>1</td><td>CLK X 4.75</td></tr><tr><td>1</td><td>1</td><td>0</td><td>CLK X 5.5</td></tr><tr><td>1</td><td>1</td><td>1</td><td>CLK X 6.0</td></tr></table>	SEL_PLL 2	SEL_PLL1	SEL_PLL0	Clock Type (MHz)	0	0	0	CLK X 4.5	0	0	1	CLK X 5.0	0	1	0	Bypass	0	1	1	CLK X 4.0	1	0	0	CLK X 4.25	1	0	1	CLK X 4.75	1	1	0	CLK X 5.5	1	1	1	CLK X 6.0
SEL_PLL 2		SEL_PLL1	SEL_PLL0	Clock Type (MHz)																																			
0		0	0	CLK X 4.5																																			
0		0	1	CLK X 5.0																																			
0		1	0	Bypass																																			
0		1	1	CLK X 4.0																																			
1		0	0	CLK X 4.25																																			
1		0	1	CLK X 4.75																																			
1		1	0	CLK X 5.5																																			
1	1	1	CLK X 6.0																																				
TSD0	117 I	O	Audio transmit serial data port 0.																																				
SEL_PLL0			Refer to the description and matrix for SEL_PLL2 pin 116.																																				
TSD1	118 I	O	Audio transmit serial data port 1.																																				
SEL_PLL1			Refer to the description and matrix for SEL_PLL2 pin 116.																																				
TSD[2:3]	120, 121	O	Audio transmit serial data ports 2 and 3.																																				
MCLK	122	I/O	Audio master clock for audio DAC.																																				
TBCK	123	O	Audio transmit bit clock.																																				
SPD_DOBM	124 I	O	S/PDIF output.																																				
SEL_PLL3			Clock source select. Strapped to VCC or ground via 4.7-kΩ resistor; read only during reset. <table><tr><th>SEL_PLL3</th><th>Clock Source</th></tr><tr><td>0</td><td>Crystal oscillator</td></tr><tr><td>1</td><td>CLK input</td></tr></table>	SEL_PLL3	Clock Source	0	Crystal oscillator	1	CLK input																														
SEL_PLL3		Clock Source																																					
0	Crystal oscillator																																						
1	CLK input																																						
SPDIF_IN	125	I	S/PDIF input; (5V tolerant input).																																				
WBLCLK	128	O	DVD-RAM wobble detector circuit clock source to preamp.																																				
WBL	129	O	DVD-RAM wobble output.																																				
LG	130	O	DVD-RAM land/groove flag.																																				
IP2	131	I	DVD-RAM header position index 2.																																				
IP1	132	I	DVD-RAM header position index 1.																																				
FLAG[3:0]	133:136	O	To monitor servo status.																																				
TEXI	139	I	High-speed tracking error input.																																				
TESTAD	140	I	Test AD input.																																				
SBAD	141	I	Sub-beam addition input signal.																																				
FEI	142	I	Focus input error signal.																																				

Table 1 ES6698 Pin Description (Continued)

Names	Pin Numbers	I/O	Definitions
AVSS_AD	143	G	Analog ground for ADC block.
CEI	144	I	Center error input signal.
TEI	145	I	Tracking error input signal.
RFRP	146	I	RF ripple/envelope input signal.
AVDD3_AD	147	P	Analog power supply for ADC block.
VREF21	148	O	2.1V reference voltage.
VREF09	149	O	0.9V reference voltage.
VREF15	150	O	1.5V reference voltage.
IREF	151	I	Servo data PLL interface reference current generator. Connect a resistor between this pin and ground to set reference current.
AVDD3_DS	152	P	Analog power supply for data slicer block.
IPIN	153	I	Inverting input of data slicer.
RFIN	154	I	Analog RF signal input after passing through equalizer (minus).
RFIP	155	I	Analog RF signal input after passing through equalizer (plus).
DSSLV	156	O	Data slicer level output.
AVSS_DS	157	G	Analog ground for data slicer block.
AVSS_PL	158	G	Analog ground for data PLL block.
PDOFTR1	159	O	Servo data PLL phase detector filter pin number 1.
FDO	160	O	Servo data PLL output node of frequency detector charge pump.
FTROPI	161	I	Servo data PLL input node of loop filter OP circuit.
AVDD3_PL	162	P	Analog power supply for data PLL block.
PLLFTR1	163	I	Servo data PLL loop filter pin number 1.
PLLFTR2	164	I	Servo data PLL loop filter pin number 2.
VREF0	165	O	Servo data PLL reference voltage output.
AWRC	166	I/O	Auto wide range control VCO signal from/to AWRC DAC.
AVSS_DA	167	G	Analog ground for DAC part.
RFRPCTR	168	I/O	Central level of RFRP.
TRAY	169	O	Output voltage level for tray buffer IC.
AVDD3_DA	170	P	Analog power supply for DAC part.
SPINDLE	171	O	Output voltage level for spindle buffer IC.
FOCUS	172	O	Output voltage level for focus buffer IC.
SLEGP	173	O	Output voltage level for Sledge buffer IC (plus).
SLEGN	174	O	Output voltage level for Sledge buffer IC (minus).
TRACK	175	O	Output voltage level for tracking buffer IC.
TESTDA	176	O	Test DA output.
FGIN	177	I	Spindle hall sensor input.

Table 1 ES6698 Pin Description (Continued)

Names	Pin Numbers	I/O	Definitions
PHOI	178	I	Sledge photo interrupt signal input.
SCSJ	179	O	Chip selection signal to RF chip (serial data enable).
SDATA	180	I/O	Data signal from/to RF chip.
SCLK	181	O	Serial clock source to RF chip.
DFCT	182	I	Defect flag input signal.
LDC	183	O	Laser diode on/off control output.
SPDON	184	O	Spindle power driver on/off control output.
GPIO[9:4]	187:192	I/O	General-purpose input/output used for servo control; (5V tolerant input).
EAUX[3:0]	193:196	I/O	Extended auxilliary ports; (5V tolerant input).
I ² C DATA	199	I/O	I ² C data I/O; (5V tolerant input).
AUX0		I/O	Auxiliary port (open collector); (5V tolerant input).
I ² C_CLK	200	I/O	I ² C clock I/O; (5V tolerant input).
AUX1		I/O	Auxiliary port (open collector); (5V tolerant input).
IOW#	201	O	I/O Write strobe (LCS1) (active-low).
HSYNC#		I/O	Horizontal sync (active-low); (5V tolerant input).
AUX2		I/O	Auxiliary port; (5V tolerant input).
IOR#	202	O	I/O Read strobe (LCS1) (active-low).
VSYNC#		I/O	Vertical sync (active-low); (5V tolerant input).
AUX3		I/O	Auxiliary port; (5V tolerant input).
C2PO	203	I	Error correction flag from CD; (5V tolerant input).
AUX4		I/O	Auxiliary port; (5V tolerant input).
AUX[5:6]	204, 205	I/O	Auxiliary ports; (5V tolerant input).
IR	206	I	Infrared remote control input; (5V tolerant input).
AUX7		I/O	Auxiliary port; (5V tolerant input).
RESET#	207	I	Reset input (active-low); (5V tolerant input).

ES6698 DEVICE INTERFACES

Table 2 lists the device interfaces for the ES6698

Table 2 ES6698 Device Interfaces

Name	Pin Numbers	I/O	Definition
Audio Port Interface	101	I	Audio receive serial data input [RSD]; (5V tolerant input).
	102	I	Audio receive bit clock input [RBCK]; (5V tolerant input).
	103	I	Audio receive frame sync input [RWS]; (5V tolerant input).
	116	O	Audio transmit frame sync output [TWS].
	117, 118, 120, 121	O	Audio transmit serial data outputs [TSD[3:0]].
	122	I/O	Audio DAC master clock [MCLK].
	123	O	Audio transmit bit clock output [TBCK].
	124	O	Sony/Philips Digital Interface audio output [SPD_DOBM].
	125	I	Sony/Philips Digital Interface audio input [SPDIF_IN]; (5V tolerant input).
Auxiliary Port Interface	193:196	I/O	Extended auxilliary ports [EAUX[3:0]]; (5V tolerant input).
	199, 200	I/O	Open collectors [AUX[1:0]]; (5V tolerant input).
	201:206	I/O	Primary auxiliary port I/Os [AUX[7:2]]; (5V tolerant input).
Clock Interface and Reset	2	I	27-MHz crystal clock input [VID_XI].
	3	O	27-MHz crystal clock output [VID_XO]
	4	I	System clock [CLK].
	29	O	DRAM clock enable output [DSCK_EN].
	51	O	Output clock [DSCK] to video memory (DRAM).
	116:118	I	Clock frequency select PLL outputs [SEL_PLL[2:0]].
	207	I	Reset input (active-low) [RESET#]; (5V tolerant input).
Display Interface	106:110, 113:115	O	Pixel data outputs [YUV[7:0]].
	201	I/O	Horizontal sync [HSYNC#].
	202	I/O	Vertical sync [VSYNC#].
EPROM/Flash ROM and RISC Port Interface	55:60, 63:69, 72:77, 80:82	O	RISC port address bus [LA[21:0]] to EPROM or Flash memory.
	83:85	O	RISC port chip select outputs [LCS[2:0]#] to EPROM or Flash memory.
	89	O	RISC port low-byte write enable output [LWRL#] to EPROM or Flash memory.
	90	O	RISC port output enable [LOE#] to EPROM and Flash memory.
	91:94, 97:100	I/O	RISC port data bus [LD[7:0]] to EPROM or Flash memory; (5V tolerant input).
Filter and Reference Voltage Interface	106	I	Video DAC reference voltage input [VREF].
	107	I	Compensation input [COMP].
Front Panel Display Interface	206	I	Infrared remote control input [IR]; (5V tolerant input).

Name	Pin Numbers	I/O	Definition
General-Purpose	187:192	I/O	General-purpose I/O [GPIO[9:4]]; (5V tolerant input).
I ² C Bus Interface	199	I/O	I ² C data I/O [I2C_DATA]; (5V tolerant input).
	200	I/O	I ² C clock I/O [I2C_CLK]; (5V tolerant input).
Power and Ground	1, 10, 19, 35, 44, 53, 62, 79, 96, 126, 185	P	I/O power supply [VD33].
	9, 18, 34, 43, 52, 61, 78, 95, 119, 127, 186, 208	G	I/O ground [VS33].
	26, 70, 86, 137, 197	G	Ground for core power [VSS].
	27, 71, 87, 138, 198	P	Core power supply [VDD].
	104	P	Power supply for PLL block. [VD33_PL].
	105	G	Ground for PLL block [VS33_PL].
	111	P	Power supply for video DAC [VD33_DA].
	112	G	Ground for video DAC [VS33_DA].
	143	G	Analog ground for ADC [AVSS_AD].
	147	P	Analog power supply for ADC [AVDD3_AD].
	152	P	Analog power supply for data slicer [AVDD3_DS].
	157	G	Analog ground for data slicer [AVSS_DS].
	158	G	Analog ground for data PLL [AVSS_PL].
	162	P	Analog power supply for data PLL [AVDD3_PL].
	167	G	Analog ground for DAC [AVSS_DA].
	170	P	Analog power supply for DAC [AVDD3_DA].
Serial Port Interface	203	I	C2PO error correction flag from CD [C2PO]; (5V tolerant input).
Servo Data Slicer Interface	153	I	Inverting input of data slicer [IPIN].
	154	I	Analog RF signal input after passing through equalizer (minus) [RFIN].
	155	I	Analog RF signal input after passing through equalizer (plus) [RFIP].
	156	O	Data slicer level output [DSSLV].

Table 2 ES6698 Device Interfaces (Continued)

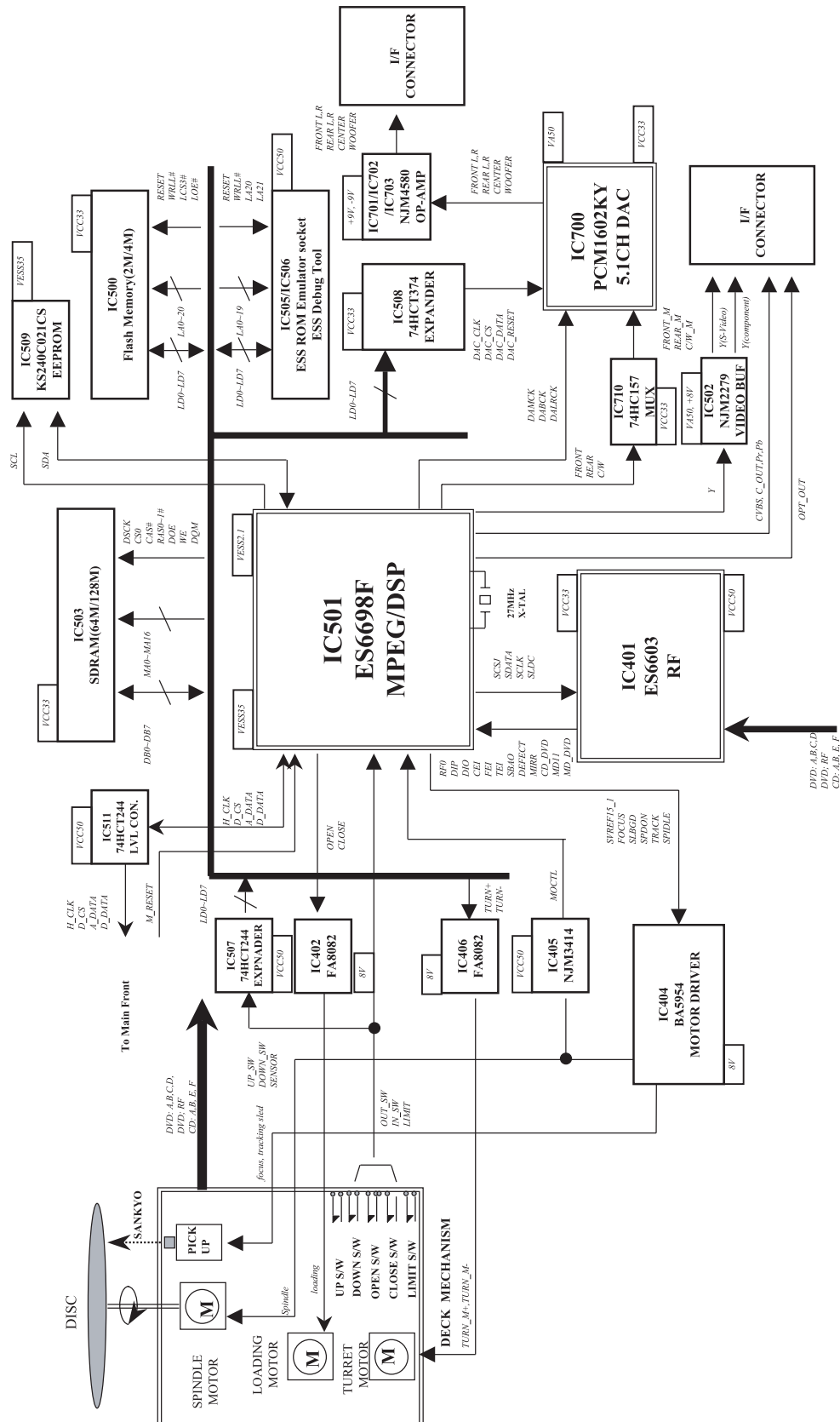
Name	Pin Numbers	I/O	Definition
Servo DAC Interface	166	I/O	Auto wide range control VCO signal from/to AWRC DAC [AWRC].
	168	I/O	Central level of RFRP [RFRPCTR].
	169	O	Output voltage level for tray buffer IC [TRAY].
	171	O	Output voltage level for spindle buffer IC [SPINDLE].
	172	O	Output voltage level for focus buffer IC [FOCUS].
	173	O	Output voltage level for Sledge buffer IC (plus) [SLEGP].
	174	O	Output voltage level for Sledge buffer IC (minus) [SLEGN].
	175	O	Output voltage level for tracking buffer IC [TRACK].
Servo Comparator Interface	176	O	Test DA output [TESTDA].
	139	I	High-speed tracking error input [TEXI].
Servo ADC Interface	140	I	Test AD input [TESTAD].
	141	I	Sub-beam addition input signal [SBAD].
	142	I	Focus input error signal [FEI].
	144	I	Center error input signal [CEI].
	145	I	Tracking error input signal [TEI].
	146	I	RF ripple/envelope input signal [RFRP].
	148	O	2.1V reference voltage [VREF21].
	149	O	0.9V reference voltage [VREF09].
Servo PLL Interface	150	I	1.5V reference voltage [VREF15].
	151	I	Servo data PLL interface reference current generator. Connect a resistor between this pin and ground to set reference current [IREF].
	159	O	Servo data PLL phase detector filter pin number 1 [PDOFTR1].
	160	O	Servo data PLL output node of frequency detector charge pump [FDO].
	161	I	Servo data PLL input node of loop filter OP circuit FTROPI].
	163	I	Servo data PLL loop filter pin number 1 [PLLFTR1].
	164	I	Servo data PLL loop filter pin number 2 [PLLFTR2].
	165	O	Servo data PLL reference voltage output [VREF0].

Table 2 ES6698 Device Interfaces (Continued)

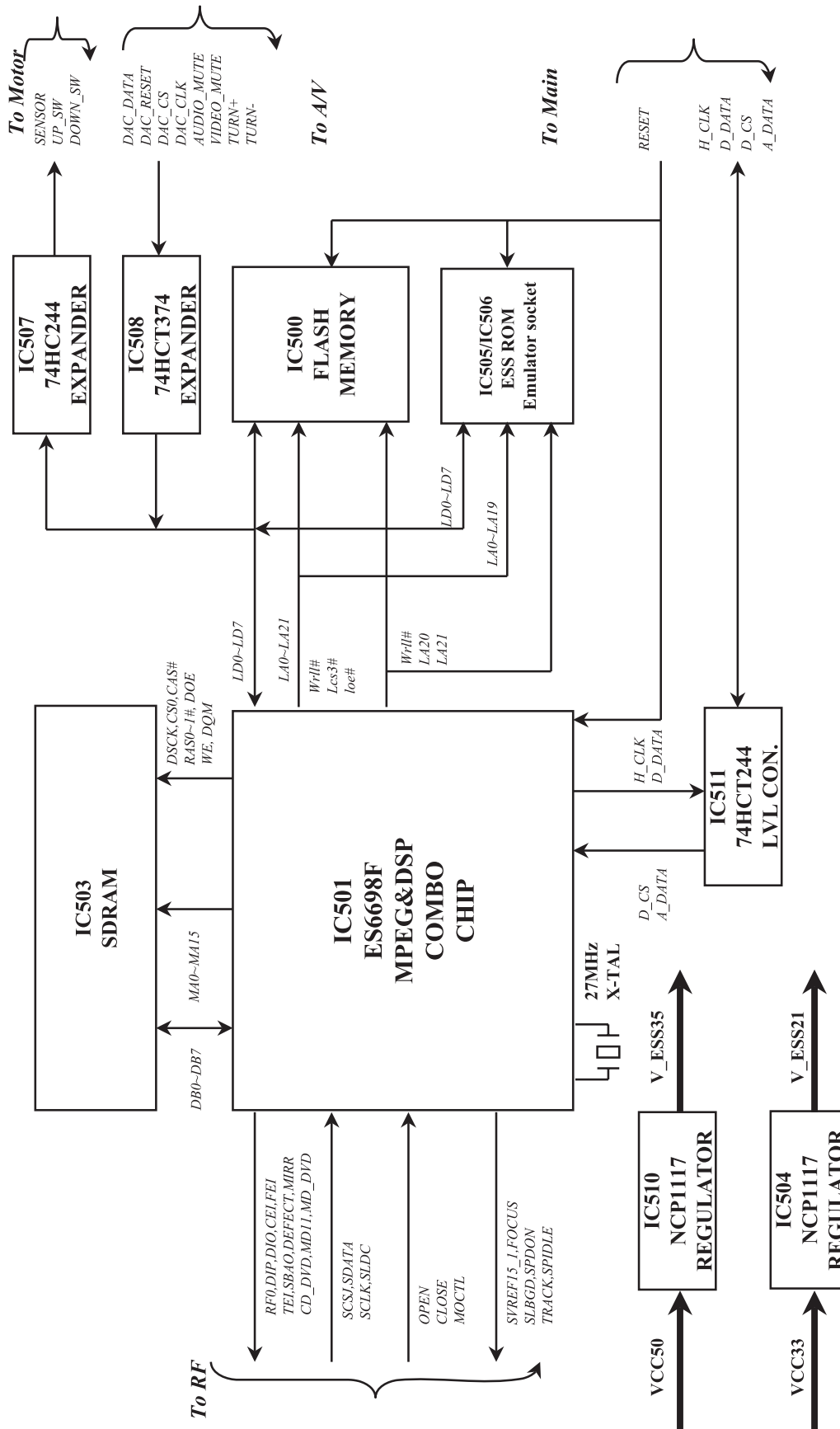
Name	Pin Numbers	I/O	Definition
Servo Control and Data Interface	133:136	O	To monitor servo status [FLAG[3:0]].
	177	I	Spindle hall sensor input [FGIN].
	178	I	Sledge photo interrupt signal input [PHOI].
	179	O	Chip selection signal to RF chip (serial data enable) [SCSJ].
	180	I/O	Data signal from/to RF chip [SDATA].
	181	O	Serial clock source to RF chip [SCLK].
	182	I	Defect flag input signal [DFCT].
	183	O	Laser diode on/off control output [LDC].
	184	O	Spindle power driver on/off control output [SPDON].
	187:192	I/O	General-purpose input/output used for servo control [GPIO[9:4]]; (5V tolerant input).
Servo DVD-RAM Interface	128	O	DVD-RAM wobble detector circuit clock source to preamp [WBLCLK].
	129	O	DVD-RAM wobble output [WBL].
	130	O	DVD-RAM land/groove flag [LG].
	131	I	DVD-RAM header position index 2 [IP2].
	132	I	DVD-RAM header position index 1 [IP1].
System Memory Interface	5:8, 11:17, 20	O	DRAM address bus [DMA[11:0]].
	21	O	Memory column address strobe output [DCAS#].
	22, 23	O	DRAM chip select outputs [DCS[1:0]#].
	24, 25, 28	O	Memory row address strobe output [DRAS[2:0]#].
	29	O	Memory output enable [DOE#].
	30	O	Memory write enable output [DWE#].
	31:33, 36:42, 45:50	I/O	Memory data bus [DB[15:0]].
	51	O	Output clock to DRAM [DSCK].
	54	O	Memory data I/O mask output [DQM].
Video DAC Interface	109	O	CVBS/chroma signal [FDAC] for simultaneous mode.
	110	O	Composite component signal [VDAC] for YUV mode.
	113	O	Luma component signal [YDAC] for YUV mode and Y/C processing.
	114	O	Chrominance component signal [CDAC] for Y/C processing.
	115	O	Chrominance component signal [UDAC] for YUV mode.

❑ DVD BLOCK DIAGRAM

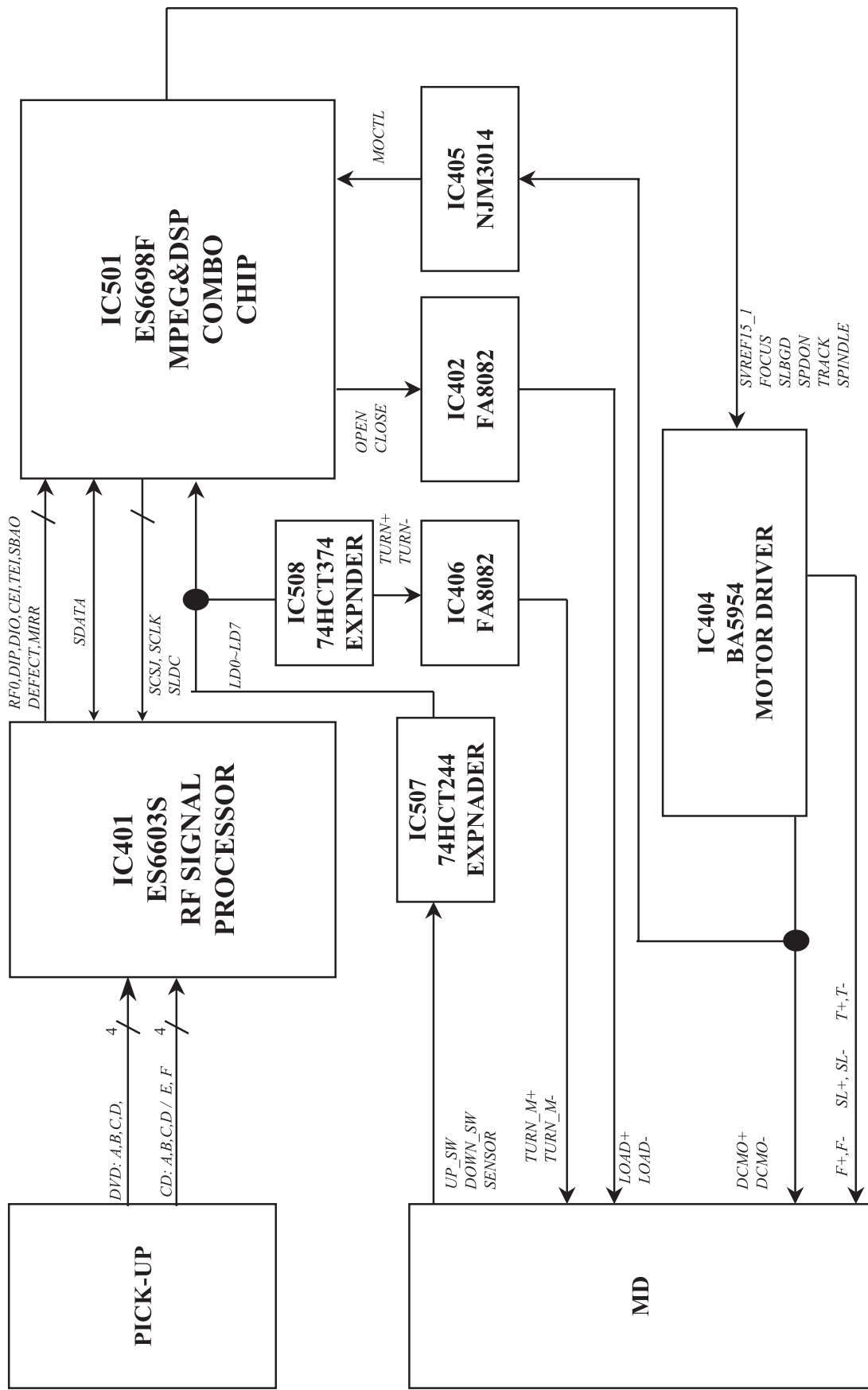
• ESS 3-CHANGER SYSTEM BLOCK DIAGRAM



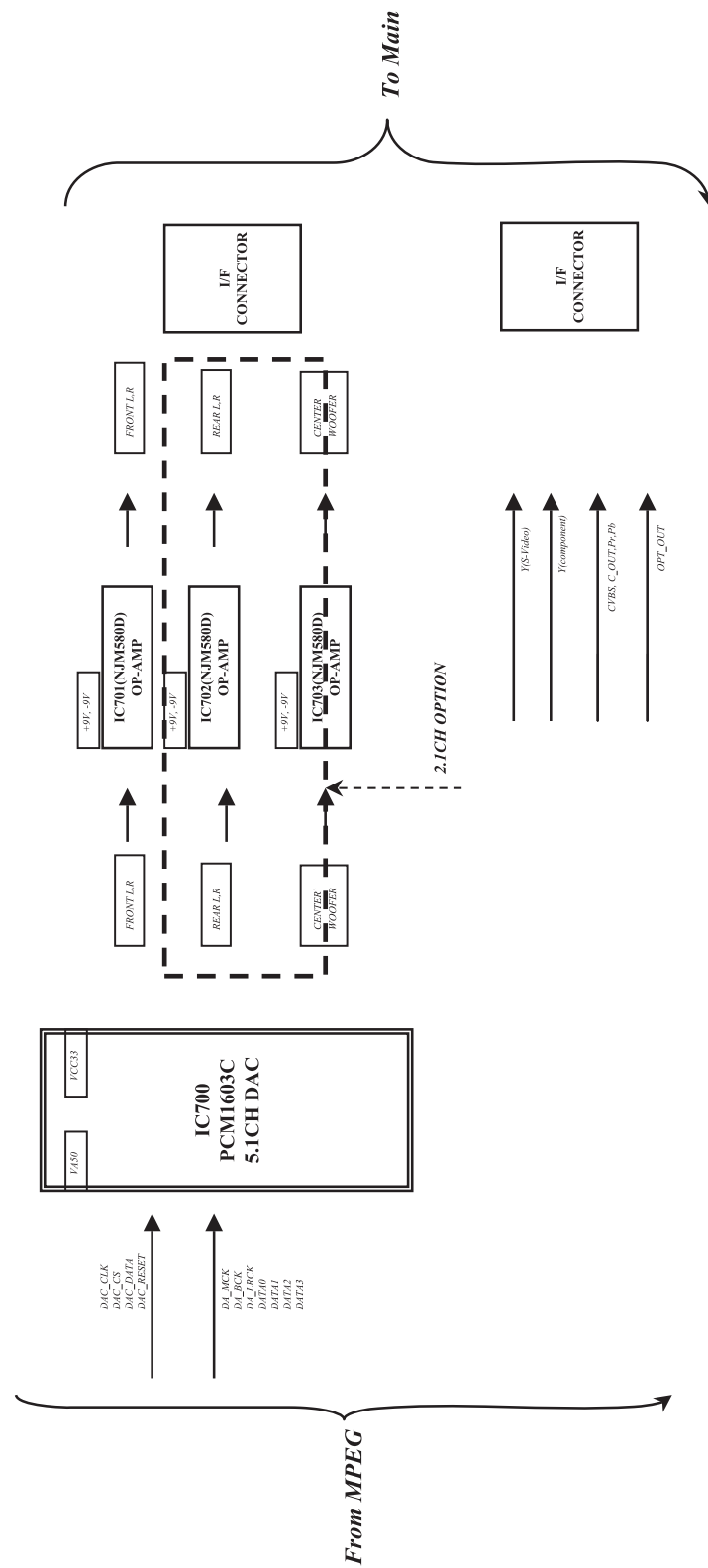
• ESS 3-CHANGER MEMORY & HOST I/F BLOCK DIAGRAM



• **ESS 3-CHANGER SERVO & MOTOR BLOCK DIAGRAM**

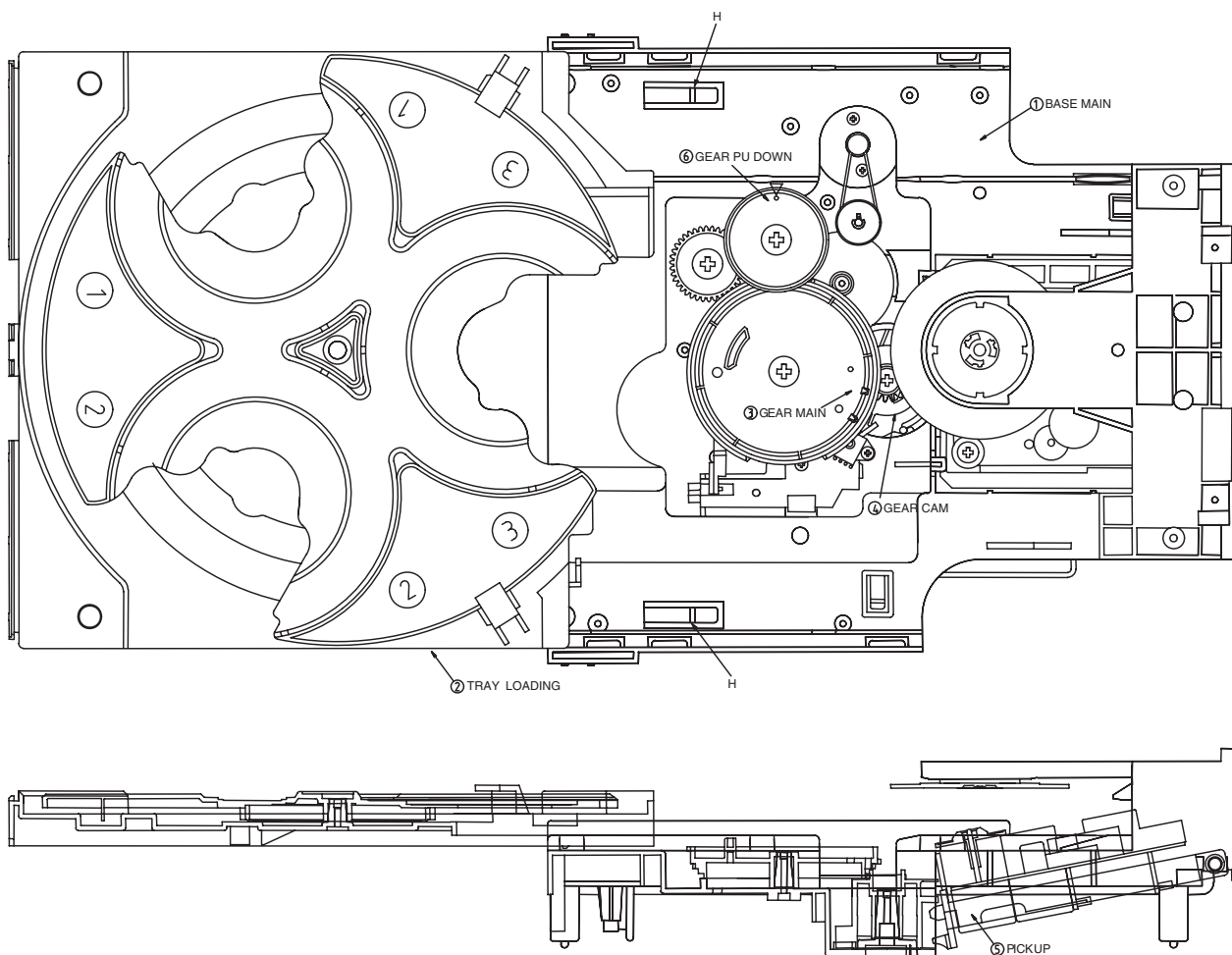


• ESS 3-CHANGER A/V SYSTEM BLOCK DIAGRAM



□ REPAIRS REGARDING CD MECHANISM

• IMPROVED MECHOD-WHEN THE TRAY GEARS WERE DISTORTED



1. How to open the tray

Push two hooks (H) of the BASE MAIN, and open the TRAY LOADING

2. How to correct the distorted gears

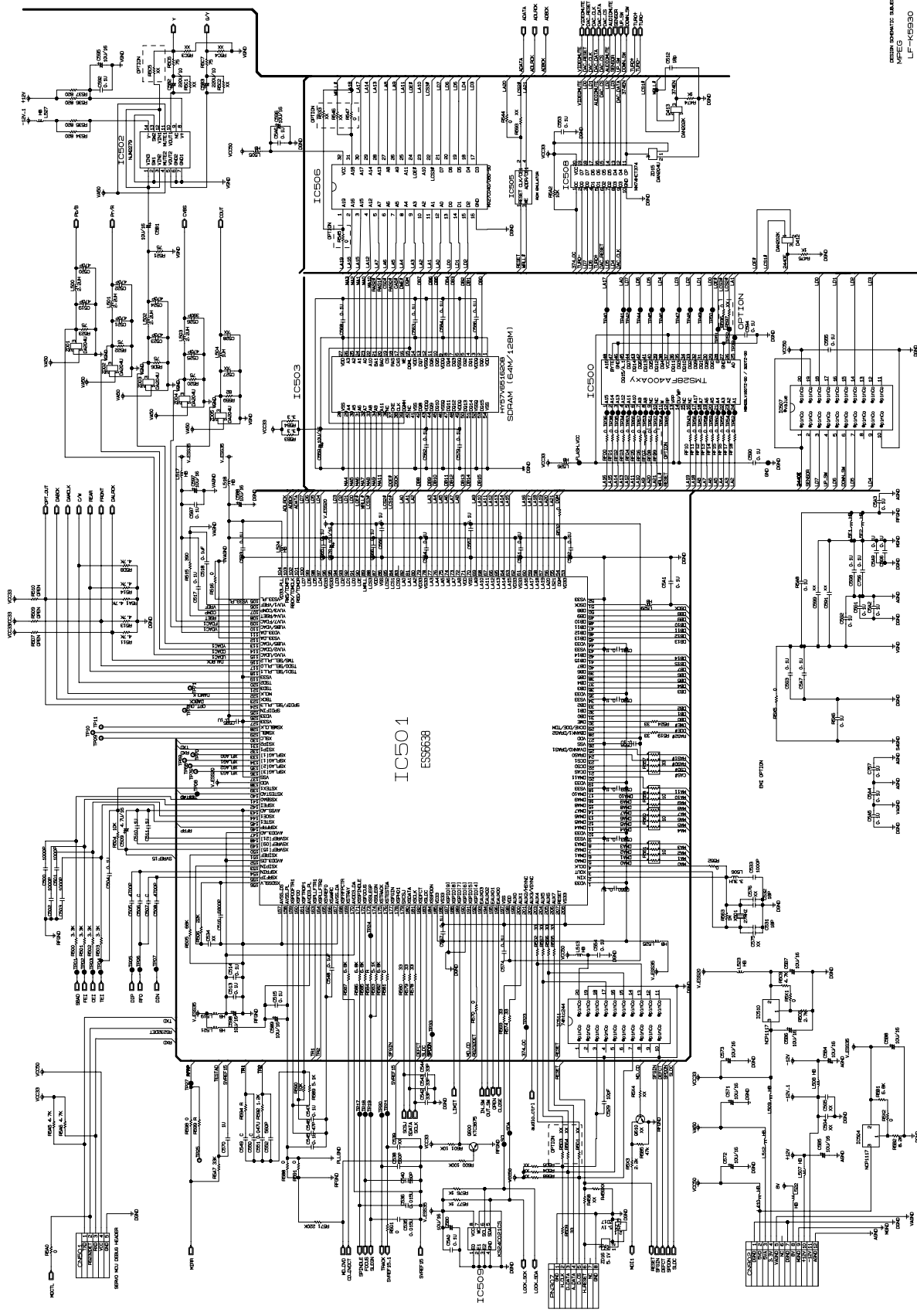
(1) Turn GEAR MAIN until it clicks, if so that PICK-UP is downed completely

(2) The hold of GEAR FU DOWN array as the arrow of BASEMAIN

(3) Push the TRAY LOADING

SCHEMATIC DIAGRAMS

- MPEG SCHEMATIC DIAGRAM



• I/O SCHEMATIC DIAGRAM

